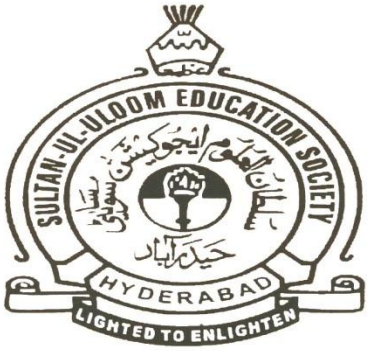
MUFFAKHAM JAH

COLLEGE OF ENGINEERING AND TECHNOLOGY

PC451EC ANALOG ELECTRONIC CIRCUITS LAB

(With effect from the academic year 2015-2016)

STUDENT'S MANUAL



DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

Vision and Mission of the Institution

Vision

To be part of universal human quest for development and progress by contributing high calibre, ethical and socially responsible engineers who meet the global challenge of building modern society in harmony with nature.

Mission

- To attain excellence in imparting technical education from the undergraduate through doctorate levels by adopting coherent and judiciously coordinated curricular and co-curricular programs
- To foster partnership with industry and government agencies through collaborative research and consultancy
- To nurture and strengthen auxiliary soft skills for overall development and improved employability in a multi-cultural work space
- To develop scientific temper and spirit of enquiry in order to harness the latent innovative talents
- To develop constructive attitude in students towards the task of nation building and empower them to become future leaders
- To nourish the entrepreneurial instincts of the students and hone their business acumen.
- To involve the students and the faculty in solving local community problems through economical and sustainable solutions.

Vision and Mission of ECE Department

Vision

To be recognized as a premier education center providing state of art education and facilitating research and innovation in the field of Electronics and Communication.

Mission

We are dedicated to providing high quality, holistic education in Electronics and Communication Engineering that prepares the students for successful pursuit of higher education and challenging careers in research, R& D and Academics.

Program Educational Objectives of B. E (ECE) Program:

1. Graduates will demonstrate technical competence in their chosen fields of employment by identifying, formulating, analyzing and providing engineering solutions using current techniques and tools
2. Graduates will communicate effectively as individuals or team members and demonstrate leadership skills to be successful in the local and global cross-cultural working environment
3. Graduates will demonstrate lifelong learning through continuing education and professional development
4. Graduates will be successful in providing viable and sustainable solutions within societal, professional, environmental and ethical contexts

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

BANJARA HILLS, ROAD NO-3, TELANGANA

LABORATORY MANUAL

FOR

ANALOG ELECTRONIC CIRCUITS LAB

Prepared by: **Checked by:**

Approved by:

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

(Name of the Subject/Lab Course): Analog Electronic Circuits

Code: EC281 **Programme: UG**

Branch: ECE **Version No: 1**

Year : II **Updated on: 20/3/16**

Semester :II **No. of Pages:**

Classification Status(Unrestricted/restricted): Unrestricted

Distribution List :Department, Lab, Library, Lab Incharge

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4) Date : **4) Date :**

Verified by: 1) Name : *** For Q.C Only**

2) Sign : **1) Name :**

3)Designation : **2) Sign :**

4) Date : **3) Designation :**

4) Date :

Approved by: (HOD) 1) Name:

2) Sign :

3) Date :

ANALOG ELECTRONIC CIRCUITS LAB

Instructions	3 Periods per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessionals	25 Marks

Objectives:

1. Verify frequency response of BJT and FET amplifiers
2. Design different negative feedback amplifiers circuits
3. Design AF and RF oscillator circuits.
4. Design power amplifiers
5. Demonstrate various circuits using PSPICE and verifying functionality.
6. Design passive filters.

Lab Experiments:

PART – A

1. Design & frequency response of single stage and multistage RC Coupled amplifier using BJT.
2. Design & frequency response of single stage and multistage RC Coupled amplifier using FET.
3. Voltage series feedback amplifier.
4. Current shunt feedback amplifier.
5. Voltage shunt feedback amplifier.
6. Current series feedback amplifier.
7. RC phase shift, Wein bridge oscillator.
8. Hartley oscillator & Colpitts Oscillator.
9. Design of Class-A power amplifier.
10. Design of Class-B power amplifier.
11. Frequency response of Tuned Amplifiers (Single and Double).
12. Transistor regulator.
13. SPICE Simulation and analysis of BJT and FET amplifier circuits.

PART – B

14. Constant K low pass and high pass filter
15. m-derived low pass and high pass filter

Suggested Reading:

1. Paul B. Zbar, Albert P.Malvino, Michael Miller, *Basic Electronics, A Text- Lab Manual*,7th ed., McGraw Hill Education (India) Private Limited,2001.
2. David Bell A, *Laboratory Manual for Electrical Circuits*, PHI-New Delhi, 2009.
3. Hayt W H Kemmerly J.E and Durbin SM, *Engineering Circuit Analysis*, 8th ed., McGraw Hill Education (India) Private Limited, 2013.

Note:

1. A total of not less than 12 experiments must be carried out during the semester. (Where ever possible, more than 1 lab experiment should be carried out in one lab session of 3 periods per week.)
2. The experiments should be performed on bread board using discrete components.
3. There should not be more than 2 students per batch while performing any of the lab experiment.

ANALOG ELECTRONICS AND INTEGRATED CIRCUITS LAB

GENERAL GUIDELINES AND SAFETY INSTRUCTIONS

1. Sign in the log register as soon as you enter the lab and strictly observe your lab timings.
2. Strictly follow the written and verbal instructions given by the teacher / Lab Instructor. If you do not understand the instructions, the handouts and the procedures, ask the instructor or teacher.
3. **Never work alone!** You should be accompanied by your laboratory partner and / or the instructors / teaching assistants all the time.
4. It is mandatory to come to lab in a formal dress and wear your ID cards.
5. Do not wear loose-fitting clothing or jewellery in the lab. Rings and necklaces are usual excellent conductors of electricity.
6. Mobile phones should be switched off in the lab. Keep bags in the bag rack.
7. Keep the labs clean at all times, no food and drinks allowed inside the lab.
8. Intentional misconduct will lead to expulsion from the lab.
9. Do not handle any equipment without reading the safety instructions. Read the handout and procedures in the Lab Manual before starting the experiments.
10. Do your wiring, setup, and a careful circuit checkout before applying power. Do not make circuit changes or perform any wiring when power is on.
11. Avoid contact with energized electrical circuits.
12. Do not insert connectors forcefully into the sockets.
13. **NEVER** try to experiment with the power from the wall plug.
14. Immediately report dangerous or exceptional conditions to the Lab instructor / teacher: Equipment that is not working as expected, wires or connectors are broken, the equipment that smells or "smokes". If you are not sure what the problem is or what's going on, switch off the Emergency shutdown.
15. Never use damaged instruments, wires or connectors. Hand over these parts to the Lab instructor/Teacher.
16. Be sure of location of fire extinguishers and first aid kits in the laboratory.
17. After completion of Experiment, return the bread board, trainer kits, wires, CRO probes and other components to lab staff. Do not take any item from the lab without permission.
18. Observation book and lab record should be carried to each lab. Readings of current lab experiment are to be entered in Observation book and previous lab experiment should be written in Lab record book. Both the books should be corrected by the faculty in each lab.
19. Handling of Semiconductor Components:Sensitive electronic circuits and electronic components have to be handled with great care. The inappropriate handling of electronic component can damage or destroy the devices. The devices can be destroyed by driving to high currents through the device, by overheating the device, by mixing up the polarity, or by electrostatic discharge (ESD). Therefore, always handle the electronic devices as indicated by the handout, the specifications in the data sheet or other documentation.
20. Special Precautions during soldering practice
    a. Hold the soldering iron away from your body. Don't point the iron towards you.
    b. Don't use a spread solder on the board as it may cause short circuit.
    c. Do not overheat the components as excess heat may damage the components/board.
    d. In case of burn or injury seek first aid available in the lab or at the college dispensary

List of Experiments

Page

EXPERIMENT NO: 1

SINGLE STAGE R-C COUPLED CE BJT AMPLIFIER

Aim:-

1. To design a single stage R-C coupled Common Emitter BJT amplifier and plot its frequency response.
2. To calculate the gain and find the cut off frequencies and Bandwidth.

Components:

Name	Quantity
Transistor BC547	1
Resistor 74KΩ, 15KΩ, 4.7KΩ, 1KΩ, 2.2KΩ, 8.2KΩ	1,1,1,1,1,1
Capacitor 10µF,100µF, 1 KPF	2, 1,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:

An amplifier is an electronic circuit that can increase the strength of a weak input signal without distorting its shape. A BJT can be used as an amplifier in the active region. The factor by which the input signal gets multiplied after passing through the amplifier circuit is called the gain of the amplifier. It is given by the ratio of the output and input signals.

Gain = output signal / input signal

A self bias circuit is used in the amplifier circuit because it provides highest Q-point stability among all the biasing circuits ie, its stability factor is the least of all. A plot of the gain of the amplifier and frequency is called the frequency response curve. The frequencies at which the gain of the amplifier is **1/√2** times the maximum value of gain are called the cutoff frequencies or 3 dB frequencies. The difference of these cutoff frequencies is called the bandwidth of the amplifier.

Bandwidth = f_H - f_L

Where **f_L** is called the lower cutoff frequency and **f_H** is called the higher cutoff frequency.

Design:

Q: Design a single stage RC coupled amplifier using a BJT in CE configuration to provide a gain of 100, lower cutoff frequency 55 Hz and an upper cutoff frequency of 55 KHz. Use BJT BC547 for which β = 200, h_{fe} = 50, h_{ie} = 1.5 KΩ and $V_{BE(active)}$ = 0.65V. The biasing conditions are as follows.V_{CC} = 12V, I_C = 1mA, V_{CE} = 6V and Stability factor is S = 10. Use R_C = 4.7KΩ.

Solution:

Use, $I_C = \beta \times I_B$

$$\Rightarrow I_B = 5\mu A$$

Apply KVL to the output loop:

$$-V_{CC} + I_C \times R_C + V_{CE} + I_C \times R_E = 0$$

$$\Rightarrow R_E = 1.3K\Omega$$

Apply Thevenin's theorem to the base circuit, then

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \text{ And } R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1+\beta}{1+\frac{\beta \times R_E}{R_B + R_E}}$$

$$\Rightarrow R_B = 12.31K\Omega$$

Apply KVL to the input loop, then

$$-V_B + I_B \times R_B + V_{BE} - I_E \times R_E = 0$$

$$\Rightarrow V_B = 2.01\text{V}$$

Divide R_B with V_B:

$$\Rightarrow R_1 = \frac{V_{CC} \times R_B}{V_B} = 73.5K\Omega$$

Also, $R_B = \frac{R_1 \times R_2}{R_1 + R_2}$ $\Rightarrow R_2 = 14.8K\Omega$

Design of R_L:-

We know that, gain $A_V = \frac{-h_{fe} \times R_L^{'}}{h_{ie}}$

$$\Rightarrow R_L^{'} = 3K\Omega$$

But, $R_L^{'} = \frac{R_L \times R_C}{R_L + R_C}$

$$\Rightarrow R_L = 8.3K\Omega$$

Design of C_E and C_{sh}:-

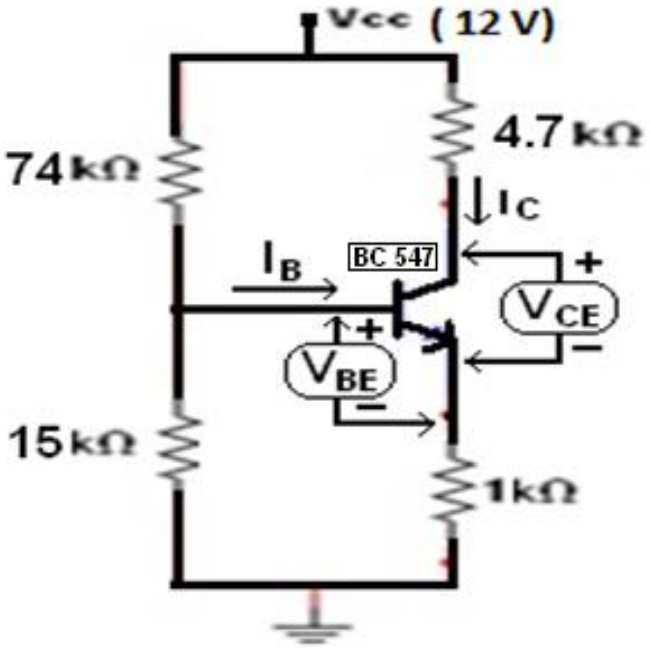
We know that $f_L = \frac{1+h_{fe}}{2\pi h_{ie} C_E}$

$$\Rightarrow C_E = 100\mu F$$

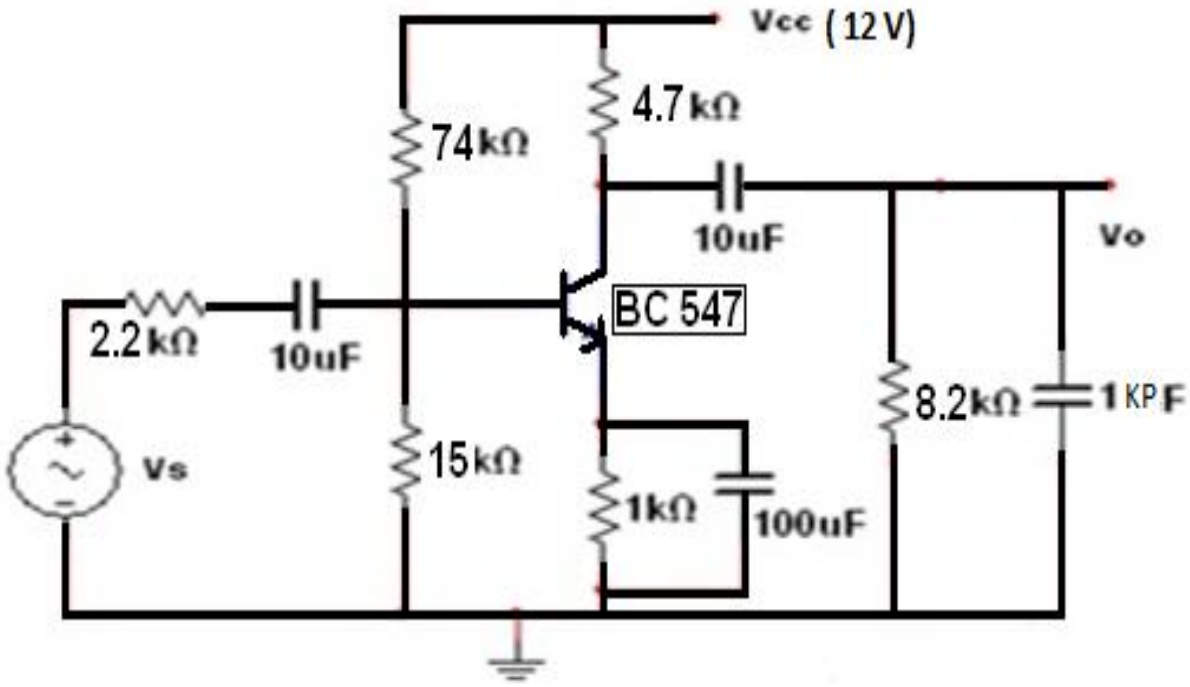
Also, $f_H = \frac{1}{2\pi R_L^{'} C_{sh}}$ $\Rightarrow C_{sh} = 1KPF$

Assume, $C_b = C_c$ = 10μF and R_S = 2.2KΩ

Circuit diagram:



Fig(1) DC bias for the BJT



Fig(2) RC Coupled CE BJT Amplifier

Procedure:

1. Connect the circuit as shown in fig 1 and obtain the DC bias conditions V_{BE}, I_B, V_{CE}, I_C.
2. Connect the circuit as shown in fig 2, Set source voltage as 30mV P-P at 1 KHz frequency using the function generator.
3. Keeping the input voltage as constant, vary the frequency from 30 Hz to 1 MHz in regular steps and note down the corresponding output P-P voltage.
4. Plot the graph for gain in (dB) verses Frequency on a semi log graph sheet.
5. Calculate the bandwidth from the graph.

Observations:

V_S = 30mV

DC conditions:

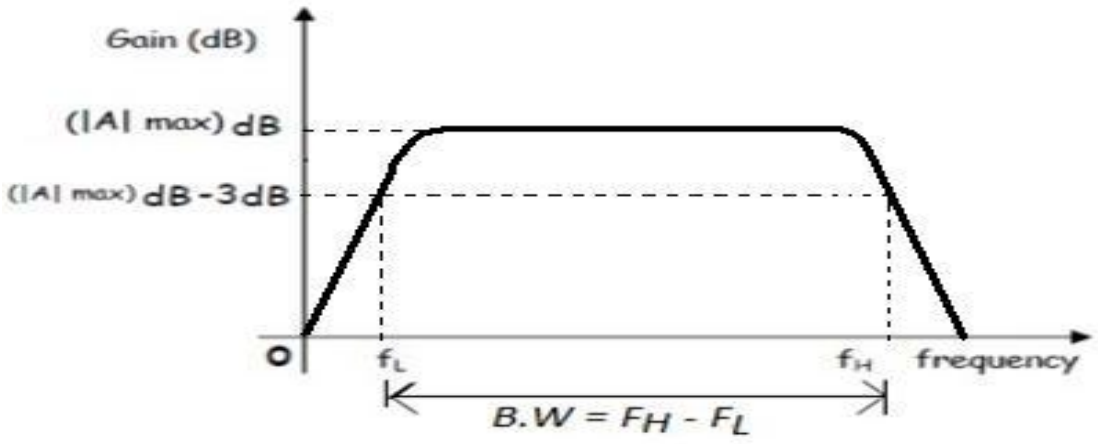
V_{BE} = ……. V_{CE} = ……

I_B = …… I_C = ……..

Frequency Response:

Frequency	Vs (Volts)	Vo(Volts)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)

Expected graph:



Fig(3) frequency response of RC Coupled CE BJT Amplifier

Result:

1. The frequency response curve of the amplifier is plotted.
2. Mid band gain, A_m = ……
3. Lower cutoff frequency, f_L = ……..
   Higher cutoff frequency, f_H = …….

   Bandwidth = $f_H - f_L$ = ……..……

EXPERIMENT NO: 2

SINGLE STAGE R-C COUPLED CS JFET AMPLIFIER

Aim:

1. To design a single stage R-C coupled Common Source JFET amplifier and plot its frequency response.
2. To find the cut off frequencies, Bandwidth and calculate its gain.

Components:

Name	Quantity
JFET BFW 11	1
Resistor 4.7KΩ, 27KΩ, 1KΩ, 1MΩ	1, 1, 1, 1
Capacitor 1µF, 10µF, 1KPF	2,1,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual power supply	0-30V	1
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	1
Connecting Wires		

Specifications:

For FET BFW11:

Gate Source Voltage V_{GS} = -30V

Forward Gain Current I_{GF} = 10mA

Maximum Power Dissipation P_D = 300mW

Theory:

An amplifier is an electronic circuit that can increase the strength of a weak input signal without distorting its shape. A JFET can be used as an amplifier in the pinch-off region. The factor by which the input signal gets multiplied after passing through the amplifier circuit is called the gain of the amplifier. It is given by the ratio of the output and input signals.

Gain = output signal / input signal

A source self bias circuit is used in the amplifier circuit. A plot of the gain of the amplifier and frequency is called the frequency response curve. The frequencies at which the gain of the amplifier is **1/√2** times the maximum value of gain are called the cutoff frequencies or 3 dB frequencies. The difference of these cutoff frequencies is called the bandwidth of the amplifier.

Bandwidth = f_H - f_L

Where **f_L** is called the lower cutoff frequency and **f_H** is called the higher cutoff frequency.

This amplifier is commonly used in buffering applications where the demand is for higher input impedance and gain is not of prime importance.

Design:

Q: Design a single stage JFET amplifier to provide a voltage gain of 10, lower cutoff frequency 50 Hz and an upper cutoff frequency of 50 KHz. Use JFET BFW10 for which I_{DSS} = 13mA, V_P = -4V, g_m = 3mS, and r_d = 20KΩ. The biasing conditions are as follows. V_{DD} = 25V, V_{DS} = 10V, I_D = 2.5mA.

Solution:

Using $I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_P}\right)^2$

$$\Rightarrow V_{GS} = V_P \times \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = -2.25V$$

Assume that R_g = 1MΩ

Apply KVL to input loop:

$$-I_G \times R_g + V_{GS} + I_D \times R_S = 0$$

But I_G = 0.

$$\Rightarrow R_S = \frac{-V_{GS}}{I_D} = 0.9K\Omega \cong 1K\Omega$$

Apply KVL to the output loop:

$$-V_{DD} + I_D \times R_D + V_{DS} + I_D \times R_S = 0$$

$$\Rightarrow R_D = 5K\Omega \cong 4.7K\Omega$$

We know that the voltage gain of a FET amplifier is given by,

$$A_V = -g_m \left(\frac{r_d \times R_L^{'}}{r_d + R_L^{'}}\right) \Rightarrow R_L = 27K\Omega$$

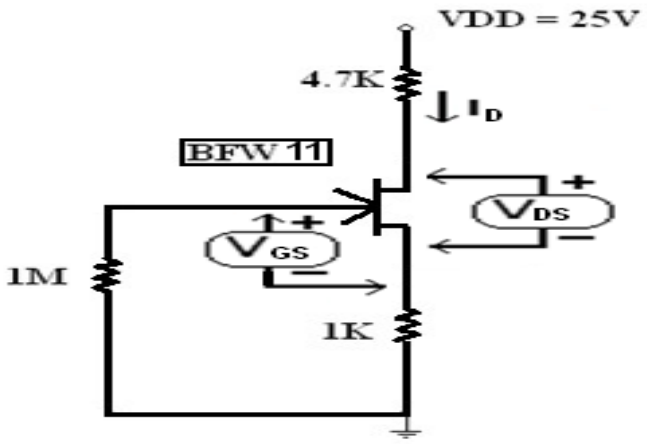
To find C_S: $$C_S = \frac{g_m}{2\pi f_L} = 10\mu F$$

To find C_{Sh}:

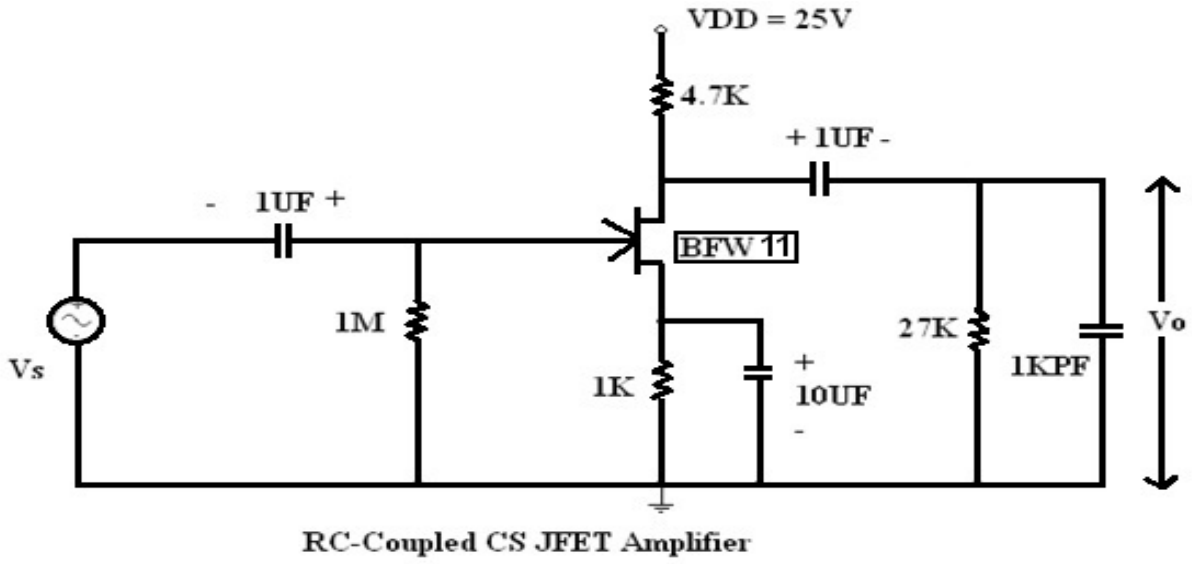
$$C_{Sh} = \frac{1}{2\pi R_L^{''} f_H} = 1nF = 1KPF$$

Apply KVL to the output loop:

Circuit diagram:



Fig(1)- DC bias of CS JFET



Fig(2)- RC Coupled CS JFET Amplifier

Procedure:

1. Connect the circuit as shown in fig 1 and obtain the DC bias conditions V_{GS}, I_G, V_{DS}, I_D.
2. Connect the circuit as shown in fig 2, Set source voltage as 50mV P-P at 1 KHz frequency using the function generator.
3. Keeping the input voltage as constant, vary the frequency from 30 Hz to 1 MHz in regular steps and note down the corresponding output P-P voltage.
4. Plot the graph for gain in (dB) verses Frequency on a semi log graph sheet.
5. Calculate the bandwidth from the graph.

Observations:

V_S = 50mV

DC conditions:-

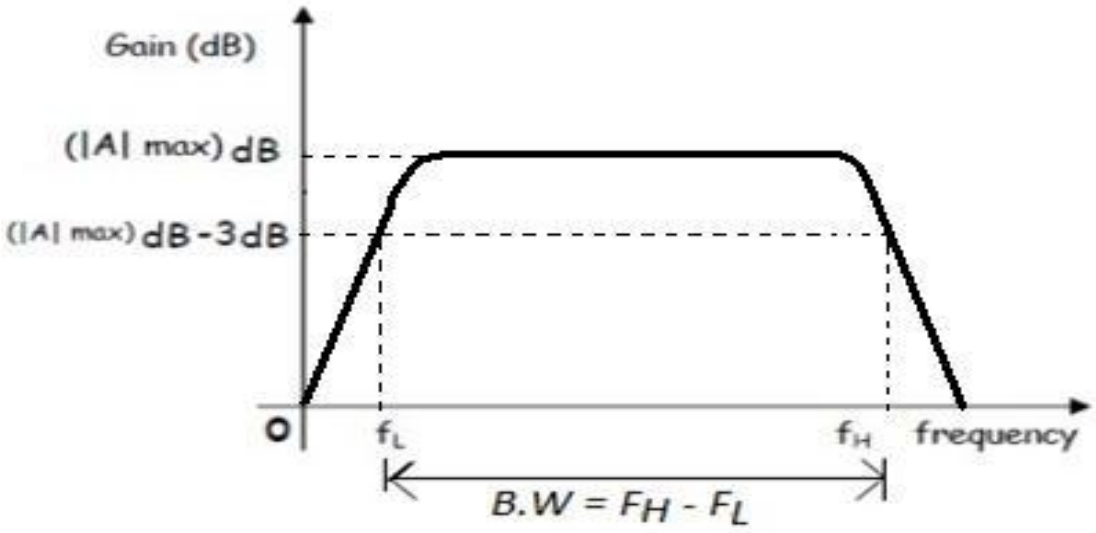
V_{GS} = ……. V_{DS} = ……

I_G = …… I_D = ……..

Frequency Response:

Frequency	Vs (Volts)	Vo(Volts)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)

Expected graph:



Fig(3)- Frequency response of RC Coupled CS JFET Amplifier

Result:

1. The frequency response curve of the amplifier is plotted.
2. Mid band gain, A_m = ……
3. Lower cutoff frequency, f_L = ……..
   Higher cutoff frequency, f_H = …….
   Bandwidth, $f_H - f_L$ = ……

EXPERIMENT NO: 3

TWO STAGE R-C COUPLED CE BJT AMPLIFIER

Aim:-

1. To design a two stage R-C coupled Common Emitter BJT amplifier and plot its frequency response.
2. To see the effect of cascading upon gain and bandwidth,

Components:

Name	Quantity
Transistor BC547	2
Resistor 100KΩ, 8.2KΩ, 820Ω, 680Ω, 120Ω, 4.7KΩ, 2.2KΩ,	2,4,1,1,1,1,1
Capacitor 10µF,100µF, 1 KPF	3, 2,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:

Cascading in amplifiers is a process of connecting the output of one amplifier to the input of the next and so on so forth. Cascading is used to increase the gain of the amplifier, but due to cascading bandwidth gets reduced.

In a multistage amplifier the overall voltage gain is the product of individual voltage gains. But the bandwidth of a multistage amplifier is always smaller than the bandwidth of individual stages.

Design:

Design a two stage amplifier to provide an overall mid band gain of 900, and a bandwidth of 55 KHz. Use BJT BC547 for which β = 250, h_{fe} = 60, h_{ie} = 1.5KΩ and $V_{BE(active)}$ = 0.65 V. The biasing conditions are V_{CC} = 20V, I_C = 1mA, V_{CE} = 11V and stability factor S = 10. Use R_C = 8.2K, R_S = 2.2K and $C_b = C_c$ = 10μF.

Design:-

Apply KVL to output loop:

$$-V_{CC} + I_C \times R_C + V_{CE} + I_C \times R_e = 0$$

$$\Rightarrow R_e = 800\Omega$$

We know that the stability factor is given by

$$S = \frac{1+\beta}{1+\frac{\beta \times R_e}{R_b + R_e}} \qquad \Rightarrow R_b = 7.69K\Omega$$

Applying KVL to the input loop:

$$-V_b + I_B \times R_b + V_{BE} - I_E \times R_e = 0$$

$$\Rightarrow V_b = 1.5V$$

Now, $$R_1 = \frac{V_{CC} \times R_b}{V_b} \cong 100K\Omega$$

Also, $$R_b = \frac{R_1 \times R_2}{R_1 + R_2} \qquad \Rightarrow R_2 = 8.2K\Omega$$

Design of R_L : To reduce the gain of first stage, split its emitter resistance into two resistors and leave one resistor un-bypassed. Assume that a gain of 7.5 is desired from the first stage. Also, the load resistor for this stage is a parallel combination of R_{C1}, R_{B2} and R_{i2}, which is equal to 1.08KΩ.

Then, $$A_{V1} = \frac{-h_{fe} \times R'_{L1}}{h_{ie} + (1+h_{fe}) \times R'_{e1}}$$

$$\Rightarrow R'_{e1} = 120\Omega$$

But, $$R_{e1} = R'_{e1} + R''_{e1}$$

$$\Rightarrow R''_{e1} = 700\Omega \cong 680\Omega$$

An overall gain of 900 is desired from the amplifier of which 7.5 is provided by first stage. Therefore the second stage must provide a gain of 120.

We know that,

$$A_{V2} = \frac{-h_{fe} \times R'_{L2}}{h_{ie}} \qquad \Rightarrow R'_{L2} = 3K\Omega$$

But, $$R'_{L2} = \frac{R_{C2} \times R_{L2}}{R_{C2} + R_{L2}} \Rightarrow R_{L2} = 4.7K\Omega$$

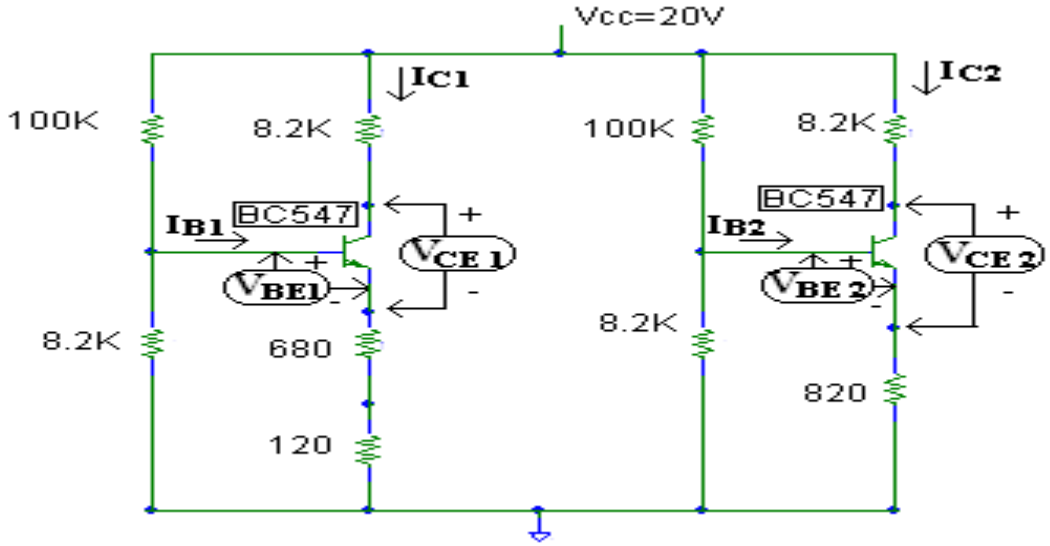
Overall bandwidth is given as 55 KHz. As the shunt capacitor is placed in the second stage, the bandwidth for first stage will be very high in comparison with that for the second stage. Therefore the overall bandwidth will be equal to the bandwidth of the second stage.

$$\therefore (BW) = (BW)_2 \cong f_{H2} = 55KHz$$

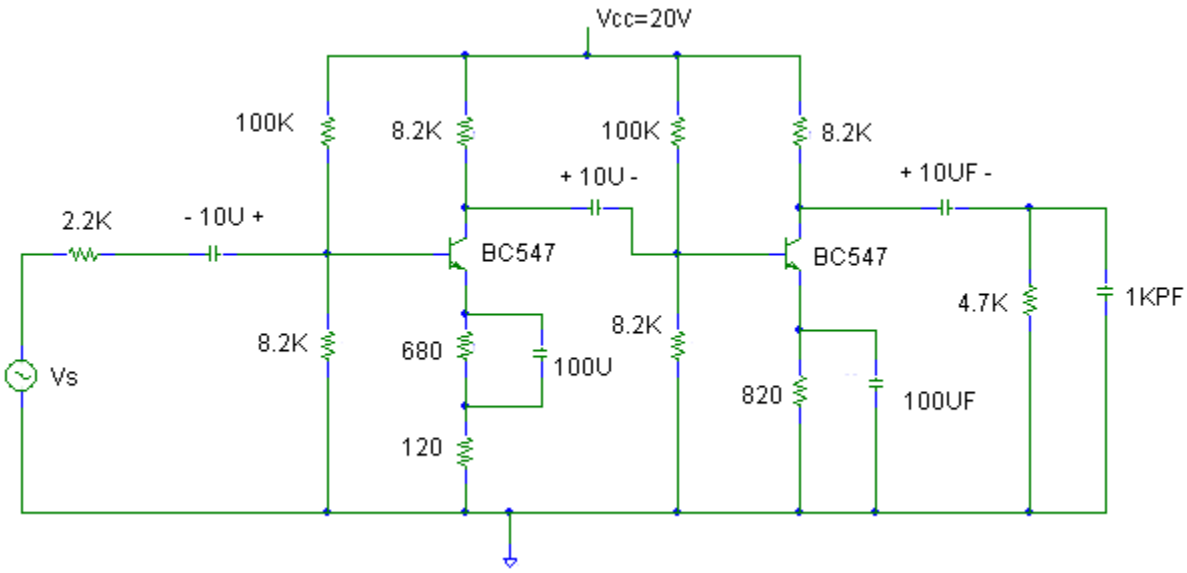
Now, $$C_{Sh} = \frac{1}{2\pi R''_{L2} f_{H2}} = 1nF = 1KPF$$

Assume the emitter bypass capacitor to be 100μF for each stage.

Circuit diagram:



Fig(1) DC bias for the BJT



Fig(2) Two stage RC Coupled CE BJT Amplifier

Procedure:

1) Connect the circuit as shown in figure1.
2) Note the DC conditions i.e, the values of base, collector currents and base to emitter, collector to emitter voltages for each stage.

3) Connect the circuit as shown in figure 2, Adjust the input signal frequency to 1 KHz and the peak to peak value of V_{i1} to 2 or 3mV. Note the peak to peak value of output voltage V_{o1} and V_{o2}. Calculate the voltage gain of each stage.

For stage-1, $A_{V1} = \frac{V_{O1}}{V_{i1}}$ For stage-2, $A_{V2} = \frac{V_{O2}}{V_{O1}}$

And overall voltage gain is, $A_V = A_{V1} \times A_{V2}$

4) Vary the frequency of the input signal from 30 Hz to 500 KHz in appropriate steps, maintain the V_{i1} constant at 2mV and note the output voltages in each step.

5) Calculate the gains A_{V1}, A_{V2}, and A_V for each value of frequency. Plot a graph between gain and frequency for each stage and the overall stage

6) Calculate bandwidth of each stage and the overall stage from the graph.

Observations:

DC conditions:

For stage-1, V_{BE1} = ……. V_{CE1} = ……

I_{B1} = …… I_{C1} = ……..

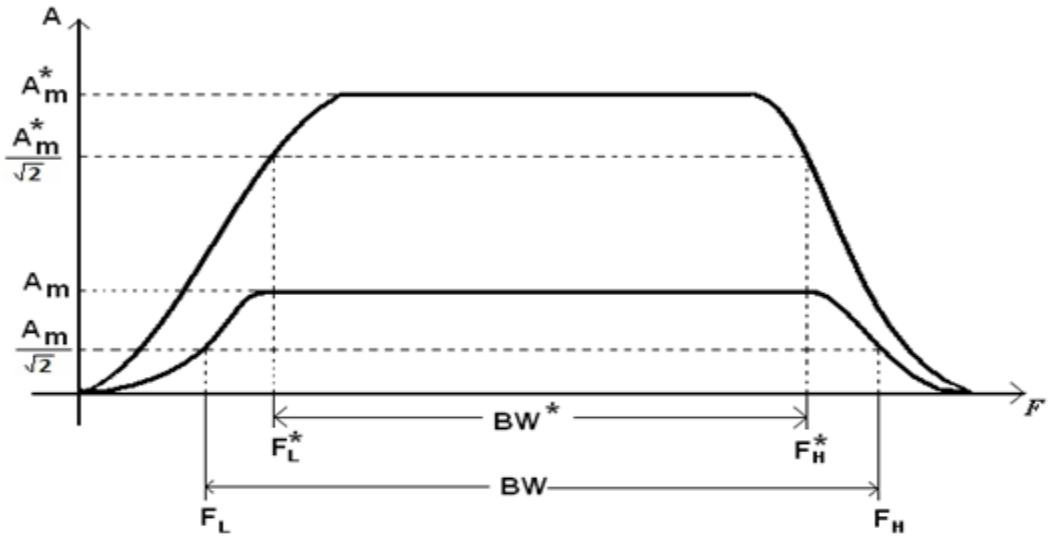
For stage-2, V_{BE2} = ……. V_{CE2} = ……

I_{B2} = …… I_{C2} = ……..

Frequency Response:

Sl.No.	Frequency	V_{i1} (mV)	V_{O1} (mV)	V_{O2} (V)	$A_{V1} = \frac{V_{O1}}{V_{i1}}$	$A_{V2} = \frac{V_{O2}}{V_{O1}}$	$A_V = A_{V1} \times A_{V2}$

Expected graph:



Fig(3) frequency response of Two stage RC Coupled CE BJT Amplifier

Result:

1) The frequency response of individual and overall stages is plotted.
2) Mid frequency gains are,

   A_{Vm1} = ……. A_{Vm2} = …… A_{Vm} = ……

3) Bandwidths are,

   BW_1 = …… BW_2 = …….. BW = ……..

4) It is observed that cascading in amplifiers increases the voltage gain but decreases the bandwidth.

EXPERIMENT NO: 4

TWO STAGE R-C COUPLED CS JFET AMPLIFIER

Aim:

1. To design a two stage R-C coupled Common Source JFET amplifier and plot its frequency response.
2. To see the effect of cascading upon gain and bandwidth

Components:

Name	Quantity
JFET BFW 11	2
Resistor 4.7KΩ, 12KΩ, 1KΩ, 1MΩ	2, 1, 2, 2
Capacitor 1µF, 10µF, 1KPF	3,2,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual power supply	0-30V	1
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	1
Connecting Wires		

Specifications:

For FET BFW11:

Gate Source Voltage V_{GS} = -30V

Forward Gain Current I_{GF} = 10mA

Maximum Power Dissipation P_D = 300mW

Theory:

Cascading in amplifiers is a process of connecting the output of one amplifier to the input of the next and so on so forth. Cascading is used to increase the gain of the amplifiers and also to get desired values of input and output impedances.

In a multistage amplifier the overall voltage gain is the product of individual voltage gains. But the bandwidth of a multistage amplifier is always smaller than the bandwidth of individual stages.

Design:

Design a two stage FET amplifier to provide an overall gain of 100, lower cutoff frequency of 75 Hz and 55 KHz. Use FET BFW10 for which g_m = 3 mS, r_d = 20 KΩ, I_{DSS} = 14 mA, and V_P = -4 V. The DC conditions are as follows. I_D = 2.5 mA, V_{DS} = 10 V and V_{DD} = 24 V.

SOL:
Using

$$I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow V_{GS} = V_P \times \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = -2.3V$$

Assume that R_g = 1MΩ

Apply KVL to input loop:

$$-I_G \times R_g + V_{GS} + I_D \times R_S = 0$$

But I_G = 0.

$$\Rightarrow R_S = \frac{-V_{GS}}{I_D} = 0.92K\Omega \cong 1K\Omega$$

Apply KVL to the output loop:

$$-V_{DD} + I_D \times R_D + V_{DS} + I_D \times R_S = 0$$

$$\Rightarrow R_D = 5K\Omega \cong 4.7K\Omega$$

For stage-1: Gain,

$$A_{V1} = -g_m \times \left(\frac{r_d \times R'_{L1}}{r_d + R'_{L1}}\right) = -11.37$$

Hence the gain for second stage is given by,

$$A_{V2} = \frac{A_V}{A_{V1}} = -8.8$$

Again,

$$A_{V2} = -g_m \times \left(\frac{r_d \times R'_{L2}}{r_d + R'_{L2}}\right) \Rightarrow R'_{L2} = 3.44K\Omega$$

$$\Rightarrow R_L = 12K\Omega$$

Design of capacitors:

Given $f_L^* = 75Hz$

And individual cutoff frequency is

$$f_L = f_L^* \times \sqrt{2^{1/n} - 1}$$

$$\Rightarrow f_L = 48.3Hz$$

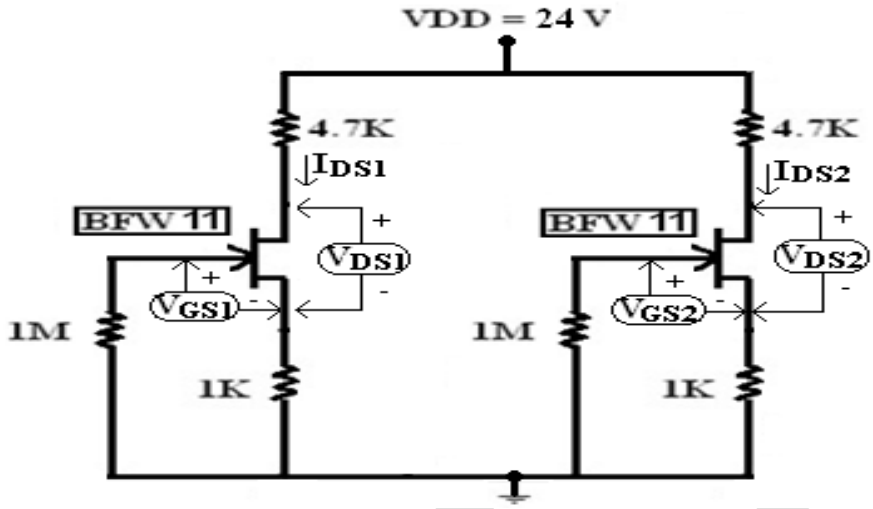
Now, $$C_S = \frac{g_m}{2\pi f_L} = 10\mu F$$

Overall higher cutoff frequency is given as 55KHz. The higher cutoff frequency for first stage will be very high in comparison with that for the second stage. Therefore the overall higher cutoff frequency will be equal to that of the second stage.

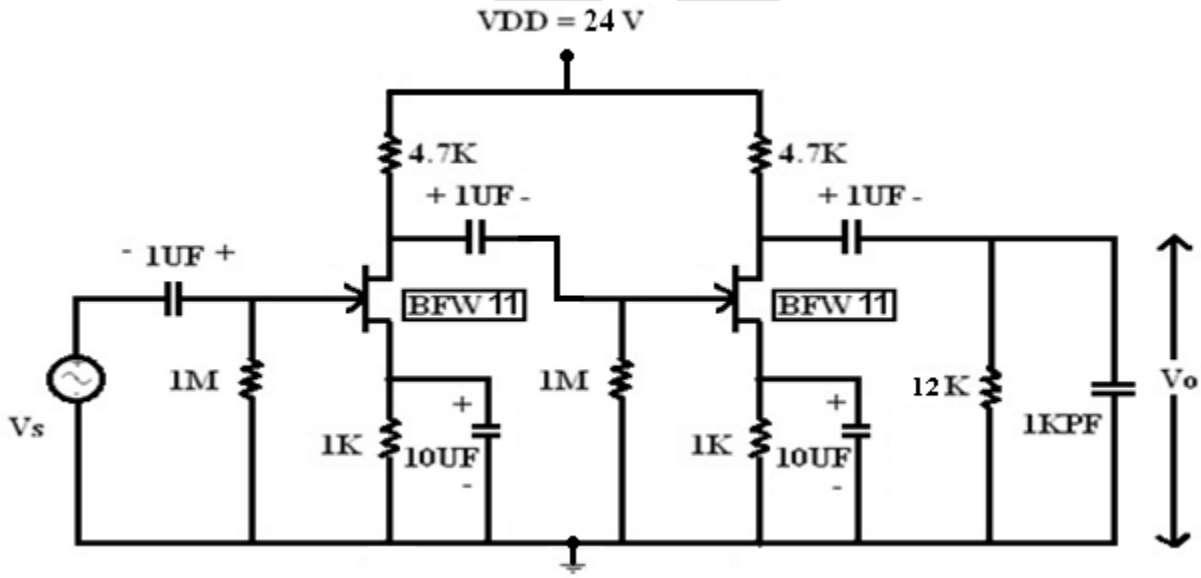
$$\therefore f_{H2} = f_H^* = 55KHz$$

Now, $$C_{Sh} = \frac{1}{2\pi R''_{L2} f_{H2}} = 1nF = 1KPF$$

Circuit diagram:



Fig(1)- DC bias of CS JFET



Fig(2)- Two stage RC Coupled CS JFET Amplifier

Procedure:

1) Connect the circuit as shown in figure1 .
2) Note the DC conditions i.e, the values of base, collector currents and base to emitter, collector to emitter voltages for each stage.

3) Connect the circuit as shown in figure 2, Adjust the input signal frequency to 1 KHz and the peak to peak value of V_{i1} to 10 mV. Note the peak to peak value of output voltage V_{o1} and V_{o2}. Calculate the voltage gain of each stage.

For stage-1, $A_{V1} = \frac{V_{O1}}{V_{i1}}$ For stage-2, $A_{V2} = \frac{V_{O2}}{V_{O1}}$

And overall voltage gain is, $A_V = A_{V1} \times A_{V2}$

4) Vary the frequency of the input signal from 30 Hz to 500 KHz in appropriate steps, maintain the V_{i1} constant at 2mV and note the output voltages in each step.

5) Calculate the gains A_{V1}, A_{V2}, and A_V for each value of frequency. Plot a graph between gain and frequency for each stage and the overall stage

6) Calculate bandwidth of each stage and the overall stage from the graph.

Observations:

DC conditions:

For stage-1, V_{GS1} = ……. V_{DS1} = …….

I_{D1} = …….

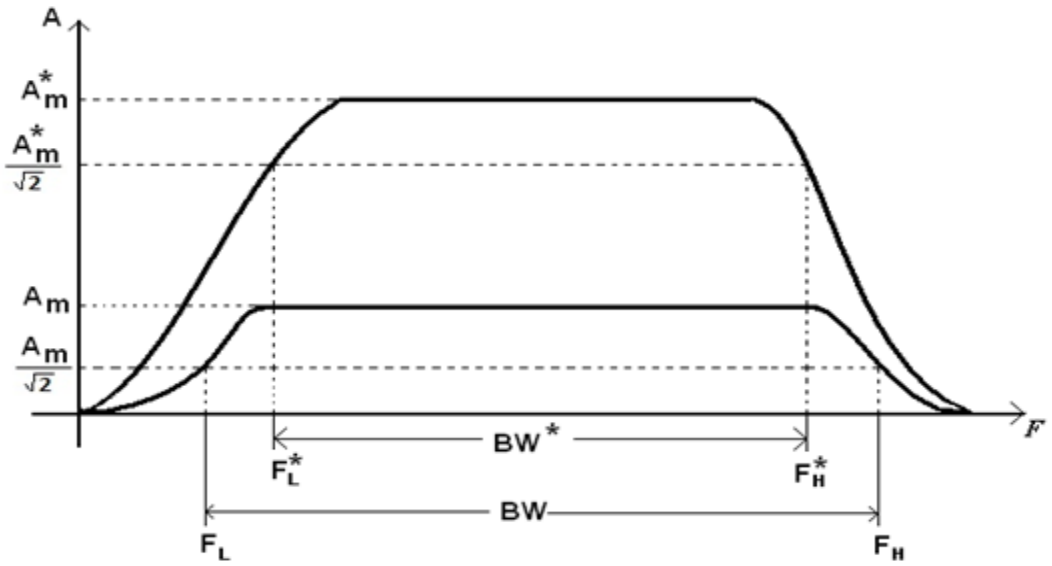
For stage-2, V_{GS2} = ……. V_{DS2} = …….

I_{D2} = …….

Frequency Response:

Sl.No.	Frequency	V_{i1} (mV)	V_{O1} (mV)	V_{O2} (V)	$A_{V1} = \frac{V_{O1}}{V_{i1}}$	$A_{V2} = \frac{V_{O2}}{V_{O1}}$	$A_V = A_{V1} \times A_{V2}$

Expected graph:



Fig(3)- Frequency response of Two stage RC Coupled CS JFET Amplifier

Result:

1) The frequency response of individual and overall stages is plotted.
2) Mid frequency gains are,

   A_{Vm1} = ……. A_{Vm2} = …… A_{Vm} = ……

3) Bandwidths are,

   BW_1 = …… BW_2 = …….. BW = ……..

4) It is observed that cascading in amplifiers increases the voltage gain but decreases the bandwidth.

EXPERIMENT NO: 5

VOLTAGE SERIES FEEDBACK AMPLIFIER

Aim:

1. To plot the frequency response of a voltage series feedback amplifier
2. To see the effect of feed back upon gain and bandwidth,

Components:

Name	Quantity
Transistor BC547	2
Resistor 100KΩ, 8.2KΩ, 820Ω, 680Ω, 120Ω, 4.7KΩ, 2.2KΩ,	2,4,1,1,1,1,1
Capacitor 10µF,100µF, 1 KPF	3, 2,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:

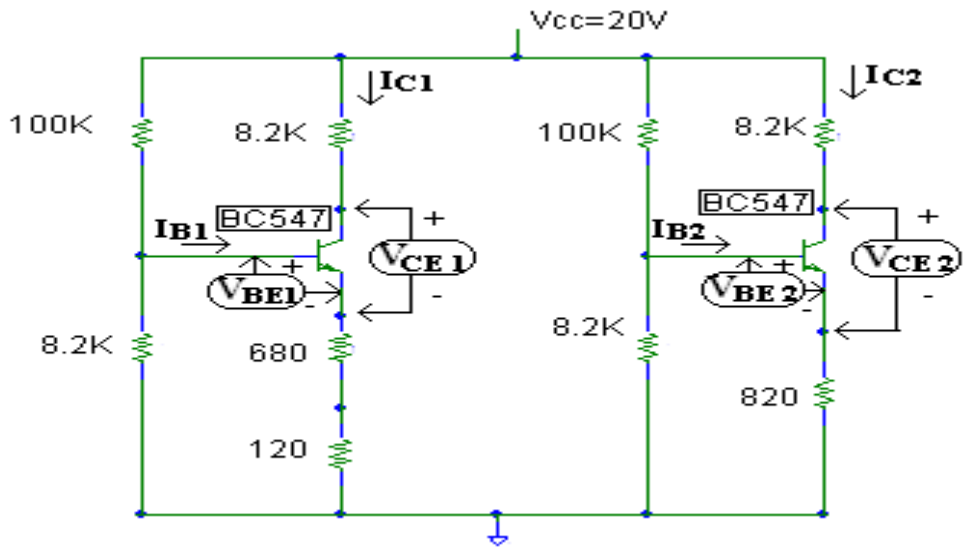
Negative feedback is defined as a process of returning a part of the output signal to the input out of phase with the input signal. It reduces gain and increases bandwidth. Negative feedback is employed in amplifier circuits to improve the stability of the gain, reduce distortion and the effect of noise. It also helps in obtaining desired values of input and output resistances.

A voltage series feedback amplifier samples output voltage and returns the feedback signal to the input in series opposing. Feedback signal is a voltage signal.

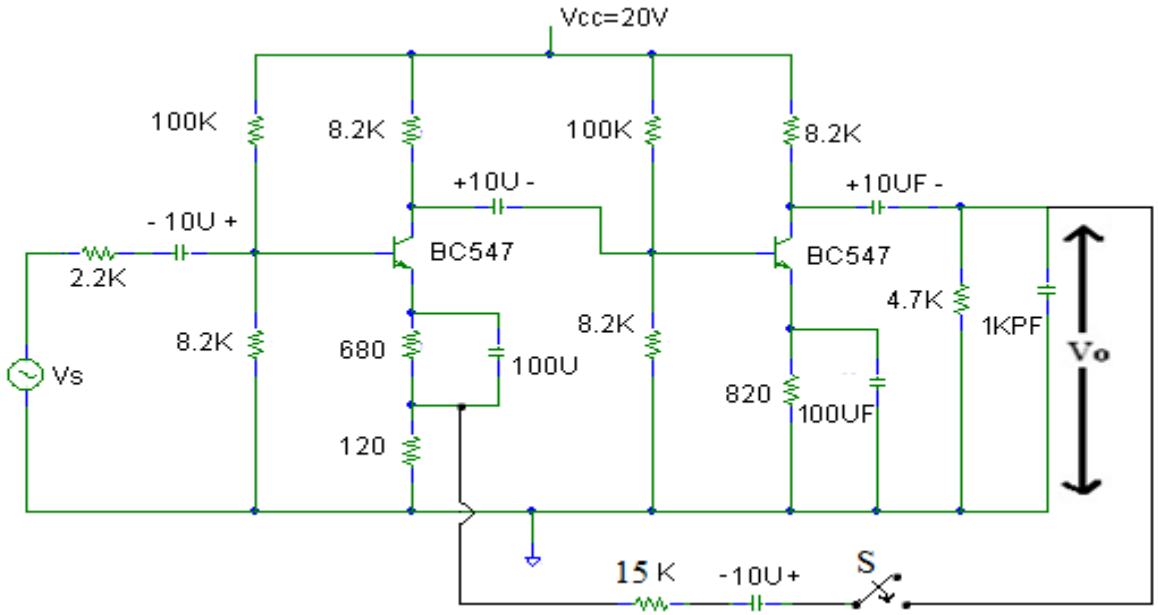
$$V_f = \beta V_O$$

Voltage series feedback increases input resistance and decreases output resistance.

Circuit diagram:



Fig(1) DC bias for the BJT



Fig(2) Voltage Series Feedback Amplifier

Procedure:

1. Connect the circuit as shown in figure 1. Note the DC conditions.
2. Connect the circuit as shown in figure 2. The switch must be open circuit, Then the circuit does not has feedback.
3. Adjust the input signal frequency to 1 KHz and the peak to peak amplitude to 3mV. Note the output voltage and calculate the gain.
4. Vary the frequency from 30 Hz to 500 KHz in appropriate steps and note V_S and V_O in each case. Calculate the gain without feedback as $A_v = \frac{V_O}{V_S}$.
5. Plot a graph between gain and frequency. Calculate bandwidth from the graph.
6. Now connect the switch as short circuit. This will introduce voltage series feedback in the circuit. Repeat steps 3 to 5. in this case vary the frequency from 30 Hz to 2 MHz.
7. Compare the gain and bandwidth with and without feedback

Observations:

DC conditions:-

For stage-1, V_{BE1} = ……. V_{CE1} = ……

I_{B1} = …… I_{C1} = ……..

For stage-2, V_{BE2} = ……. V_{CE2} = ……

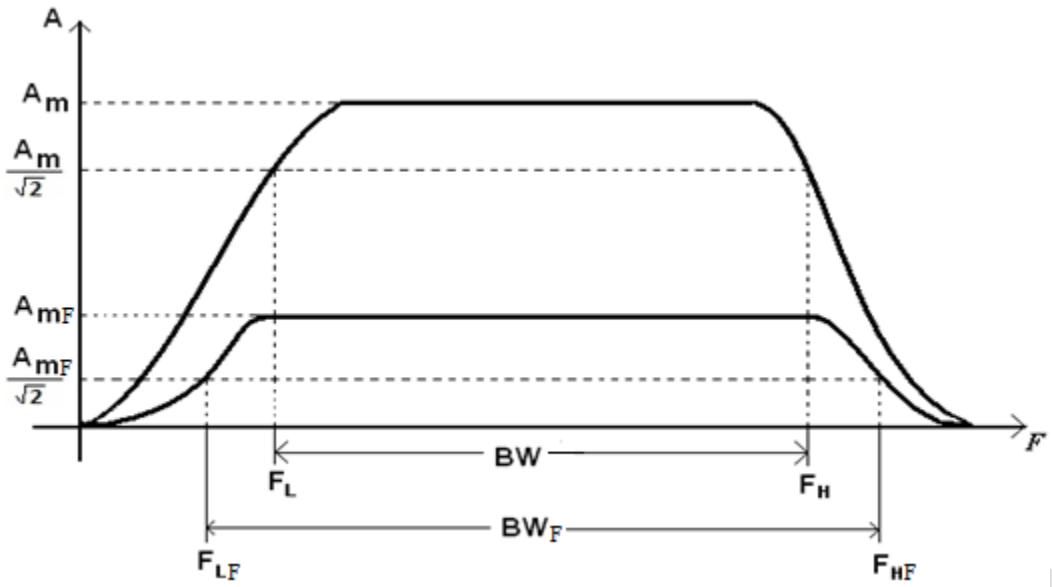
I_{B2} = …… I_{C2} = ……..

Frequency Response:-

Frequency Response:

Sl.No.	Frequency	V_i (mV)	V_O (V)	$V_{O\,f}$ (V)	$A_V = \frac{V_O}{V_i}$	$A_{V\,f} = \frac{V_{O\,f}}{V_i}$

Expected graph:



Fig(3) Frequency response of Voltage Series Feedback Amplifier

Result:

Gain without feedback = ----------

Bandwidth without feedback = ----------

Gain with feedback = ----------

Bandwidth with feedback = ----------

EXPERIMENT NO: 6

CURRENT SHUNT FEEDBACK AMPLIFIER

Aim:

1. To plot the frequency response of a current shunt feedback amplifier
2. To see the effect of feed back upon gain and bandwidth,

Components:

Name	Quantity
Transistor BC547	2
Resistor 100KΩ, 8.2KΩ, 820Ω, 680Ω, 120Ω, 4.7KΩ, 2.2KΩ,	2,4,1,1,1,1,1
Capacitor 10µF,100µF, 1 KPF	3, 2,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:

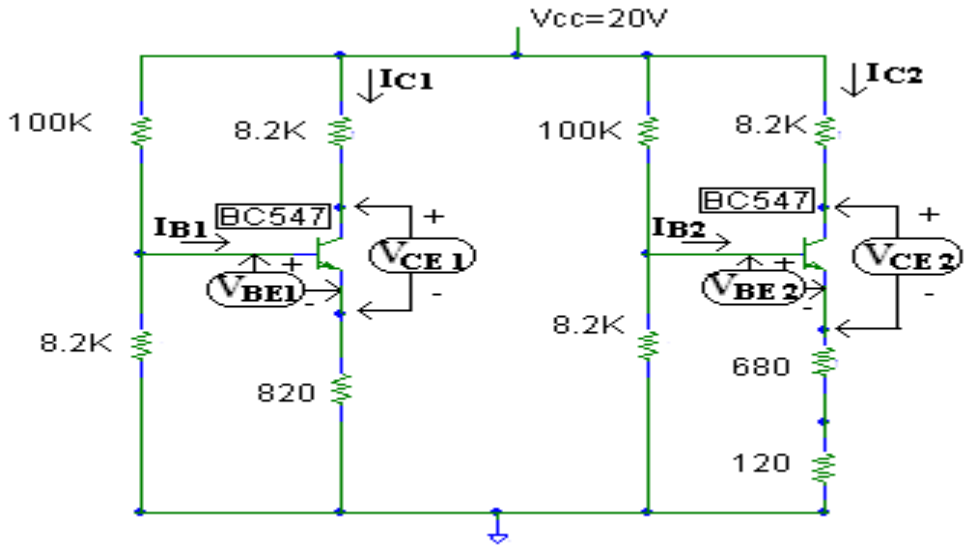
Negative feedback is defined as a process of returning a part of the output signal to the input out of phase with the input signal. It reduces gain and increases bandwidth. Negative feedback is employed in amplifier circuits to improve the stability of the gain, reduce distortion and the effect of noise. It also helps in obtaining desired values of input and output resistances.

A current shunt feedback amplifier samples output current and returns the feedback signal to the input in shunt. Feedback signal is a voltage signal.

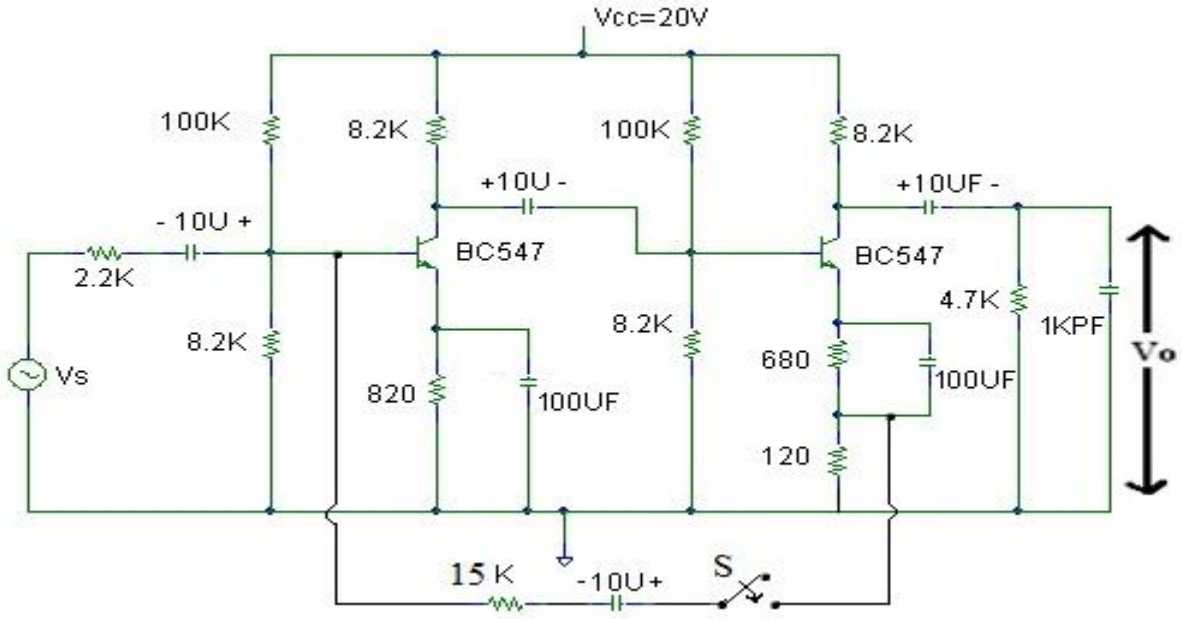
$$I_f = \beta I_L$$

Current shunt feedback increases output resistance and decreases input resistance.

Circuit diagram:



Fig(1) DC bias for the BJT



Fig(2) Current Shunt Feedback Amplifier

Procedure:

1. Connect the circuit as shown in figure 1. Note the DC conditions.
2. Connect the circuit as shown in figure 2. The switch must be open circuit, Then the circuit does not has feedback.
3. Adjust the input signal frequency to 1 KHz and the peak to peak amplitude to 3mV. Note the output voltage and calculate the gain.
4. Vary the frequency from 30 Hz to 500 KHz in appropriate steps and note V_S and V_O in each case. Calculate the gain without feedback as $A_v = \frac{V_O}{V_S}$.
5. Plot a graph between gain and frequency. Calculate bandwidth from the graph.
6. Now connect the switch as short circuit. This will introduce current shunt feedback in the circuit. Repeat steps 3 to 5. in this case vary the frequency from 30 Hz to 2 MHz.
7. Compare the gain and bandwidth with and without feedback

Observations:

DC conditions:

For stage-1, V_{BE1} = ……. V_{CE1} = ……

I_{B1} = …… I_{C1} = ……..

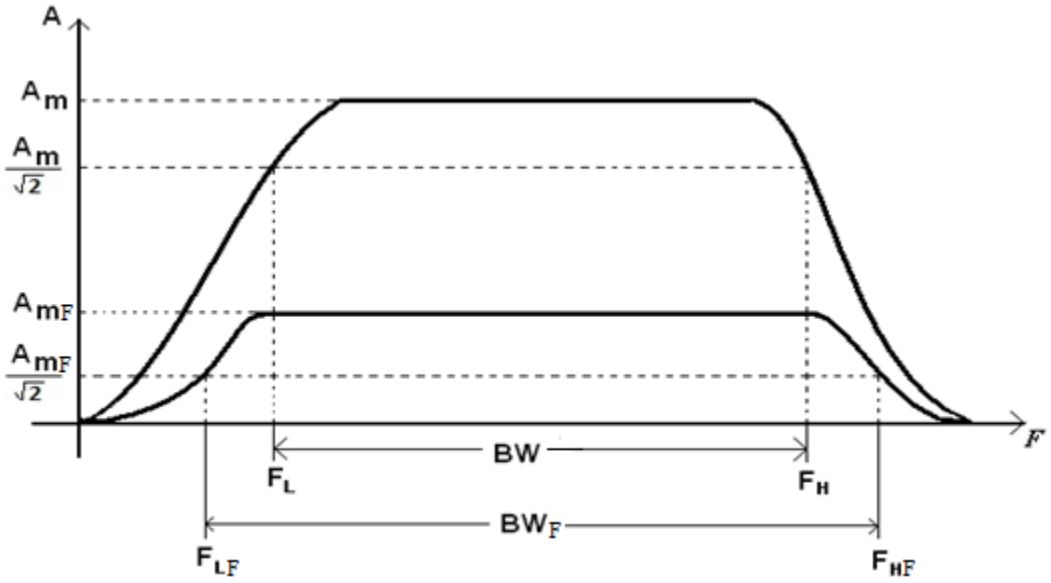
For stage-2, V_{BE2} = ……. V_{CE2} = ……

I_{B2} = …… I_{C2} = ……..

Frequency Response:

Sl.No.	Frequency	V_i (mV)	V_O (V)	$V_{O\,f}$ (V)	$A_V = \frac{V_O}{V_i}$	$A_{V\,f} = \frac{V_{O\,f}}{V_i}$

Expected graph:



Fig(3) frequency response of Current Shunt Feedback Amplifier

Result:

Gain without feedback = ----------

Bandwidth without feedback = ----------

Gain with feedback = ----------

Bandwidth with feedback = ----------

EXPERIMENT NO : 7

RC PHASE-SHIFT OSCILLATOR

Aim:

To design and study the operation of RC Phase-shift Oscillator using BJT and verify Barkhausen's criterion.

Components:

Name	Quantity
Transistor BC547	1
Resistor 74KΩ, 15KΩ, 4.7KΩ, 1KΩ, 6.8K,2.2K	1,1,2,1,2,1
Capacitor 10µF,100µF, 1 KPF	2, 1,3

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:-

An oscillator is an electronic circuit that provides an AC output without using any AC input. All Sinusoidal oscillator circuits use the concept of positive feedback to produce oscillations. An oscillator circuit must satisfy the Barkhausen's criterion of unity loop gain to produce oscillations.

The Common Emitter amplifier provides a phase shift of 180˚. Additional 180˚ of phase shift required to satisfy the Barkhausen's criterion of phase shift is provided by the RC phase-shifting network. RC Phase-shift oscillator is used at Audio Frequencies.

Design:

Q: Design RC Phase-shift oscillator circuit to provide oscillations at a frequency of 8 KHz. Use BJT BC547 for which β = 200, h_{fe} = 50, h_{ie} = 1.5 KΩ and $V_{BE(active)}$ = 0.65V. The biasing conditions are as follows.V_{CC} = 12V, I_C = 1mA, V_{CE} = 6V and Stability factor is S = 10.
Use $R_C = 4.7K\Omega$.

Solution:

Use, $I_C = \beta \times I_B$

$$\Rightarrow I_B = 5\mu A$$

Apply KVL to the output loop:

$$-V_{CC} + I_C \times R_C + V_{CE} + I_C \times R_E = 0$$

$$\Rightarrow R_E = 1.3K\Omega$$

Apply Thevenin's theorem to the base circuit, then

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \text{ And } R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1+\beta}{1+\frac{\beta \times R_E}{R_B + R_E}}$$

$$\Rightarrow R_B = 12.31K\Omega$$

Apply KVL to the input loop, then

$$-V_B + I_B \times R_B + V_{BE} - I_E \times R_E = 0$$

$$\Rightarrow V_B = 2.01\text{V}$$

Divide R_B with V_B:

$$\Rightarrow R_1 = \frac{V_{CC} \times R_B}{V_B} = 73.5K\Omega$$

Also, $R_B = \frac{R_1 \times R_2}{R_1 + R_2} \quad \Rightarrow R_2 = 14.8K\Omega$

We know that $f_o = \frac{1}{2\pi \times RC\sqrt{6+4K}}$

where $K = \frac{R_C}{R}$

Assume that $R = 6.8K\Omega$. Then $C = 1KPF$.

Also $R_3 + h_{ie} = R \quad \Rightarrow R_3 = 4.7K\Omega$

Circuit diagram:-

For Part-I:

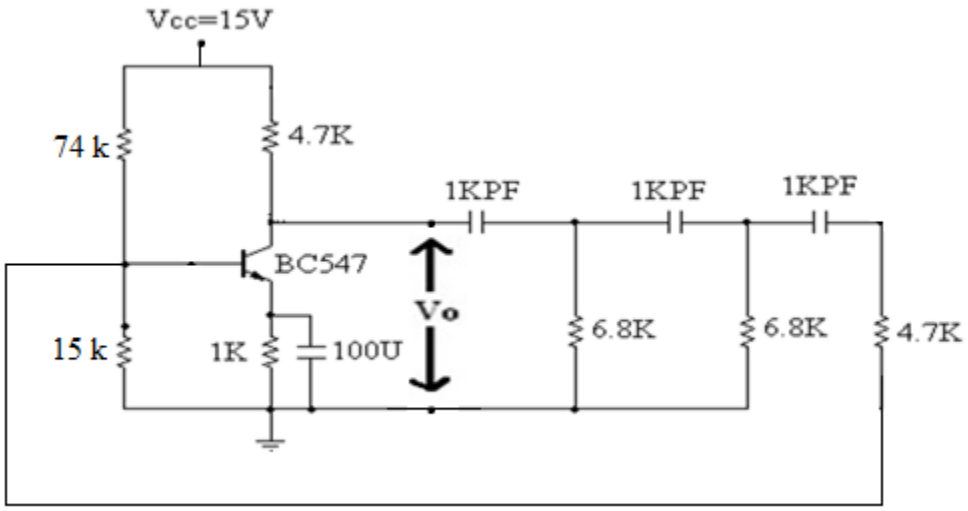


Fig (1) : RC Phase shift oscillator

For Part-II:

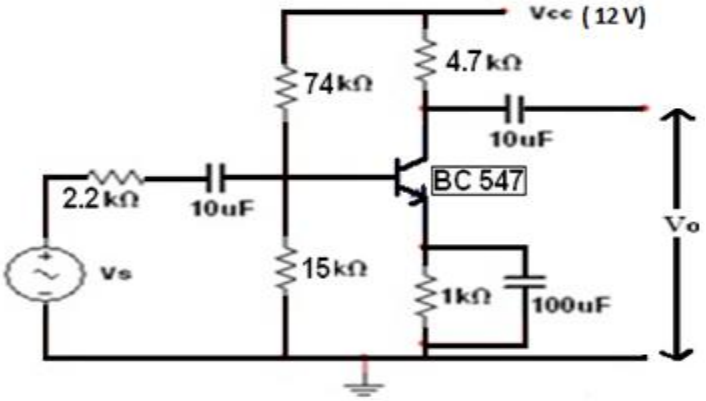


Fig (2): Amplifier Circuit diagram

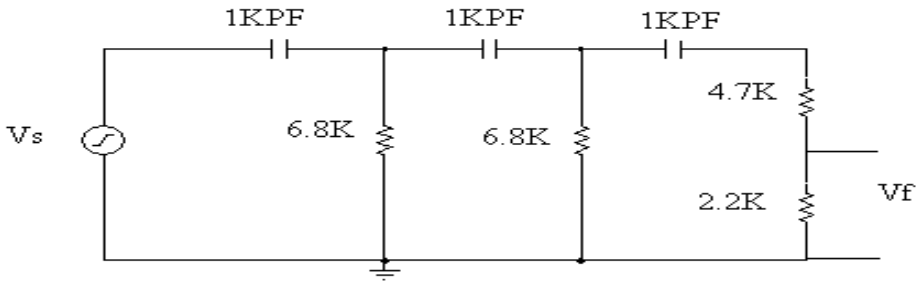


Fig (3): Feedback network

Procedure:-

Part-I: Study of operation

1) Connect the self bias circuit and check the DC conditions.
2) Connect other components of the oscillator circuit as shown in figure. Observe the output voltage waveform on CRO screen. Note down its peak to peak amplitude and frequency.

Part-II: Verification of Barkhausen's criterion

1) Connect only the amplifier circuit and find its gain at the frequency of oscillations. Apply an input of 30mV. Also observe the phase shift between input and output voltages.
2) Connect only the feedback network as shown and compute the feedback factor β as $\beta = \frac{V_f}{V_S}$.
3) Compute the loop gain as $A \times \beta$. This product should be greater than or equal to unity.
4) Observe the phase shift between V_f and V_S.
5) Add the phase shift provided by the amplifier and feedback network. The sum should be equal to 360˚.

Observations: -

Draw the output waveform; mark its peak-to-peak amplitude and time period.

Result:-

Frequency of oscillations, f_o = ----------

Peak to peak amplitude of output = ----------

Loop gain = ----------

Phase shift = ----------

Hence Barkhausen's criterion is satisfied.

EXPERIMENT NO: 8

COLPITTS OSCILLATOR

Aim:

To design and study the operation of colpitts Oscillator using BJT and determine the frequency of oscillation.

Components:

Name	Quantity
Transistor BC547	1
Resistor 74KΩ, 15 KΩ, 4.7KΩ, 1KΩ,	1,1,1,1
Capacitor 4.7µF, 1 KPF	2, 1
Inductor 70 µH	1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:-

An oscillator is an electronic circuit that provides an AC output without using any AC input. All Sinusoidal oscillator circuits use the concept of positive feedback to produce oscillations. An

oscillator circuit must satisfy the Barkhausen's criterion of unity loop gain to produce oscillations.

Colpitt's oscillator is a popular LC Oscillator circuit used at Radio Frequencies.

Design:

Q: Design Colpitt's oscillator circuit to provide oscillations at a frequency of 850 KHz. Use BJT BC547 for which β = 200, h_{fe} = 50, h_{ie} = 1.5 KΩ and $V_{BE(active)}$ = 0.65V. The biasing conditions are as follows.V_{CC} = 12V, I_C = 1mA, V_{CE} = 6V and Stability factor is S = 10. Use R_C = 4.7KΩ.

Solution:

Use, $I_C = \beta \times I_B$

$$\Rightarrow I_B = 5\mu A$$

Apply KVL to the output loop:

$$-V_{CC} + I_C \times R_C + V_{CE} + I_C \times R_E = 0$$

$$\Rightarrow R_E = 1.3K\Omega$$

Apply Thevenin's theorem to the base circuit, then

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \text{ And } R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1+\beta}{1+\frac{\beta \times R_E}{R_B + R_E}}$$

$$\Rightarrow R_B = 12.31K\Omega$$

Apply KVL to the input loop, then

$$-V_B + I_B \times R_B + V_{BE} - I_E \times R_E = 0$$

$$\Rightarrow V_B = 2.01\text{V}$$

Divide R_B with V_B:

$$\Rightarrow R_1 = \frac{V_{CC} \times R_B}{V_B} = 73.5K\Omega$$

Also, $R_B = \frac{R_1 \times R_2}{R_1 + R_2} \Rightarrow R_2 = 14.8K\Omega$

We know that $f_o = \frac{1}{2\pi} \times \sqrt{\frac{1}{L}(\frac{1}{C_1} + \frac{1}{C_2})}$

Assume that $C_1 = C_2 = 1KPF$. Then $L = 70\mu H$

Circuit diagram:-

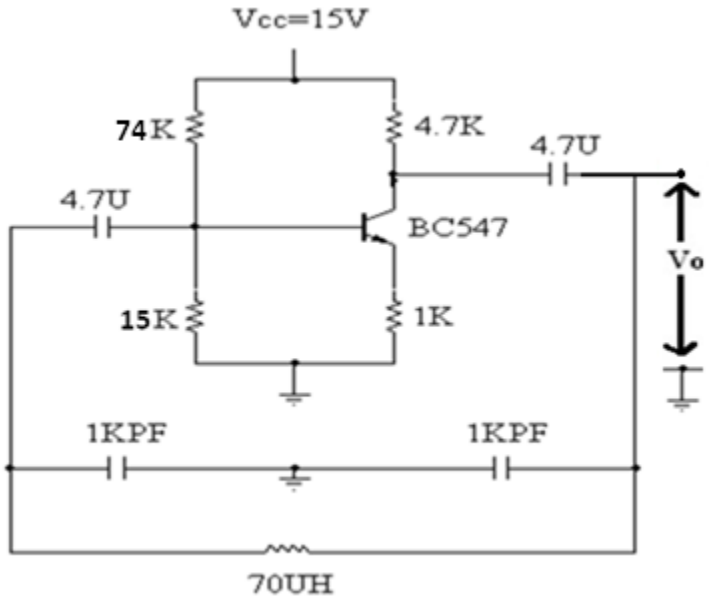


Fig (1): Colpitts Oscillator

Procedure:-

1) Connect the self bias circuit and check the DC conditions.
2) Connect other components of the oscillator circuit as shown in figure 1. Adjust the capacitance to 800 PF.
3) Observe the output voltage waveform on CRO screen. Note down its peak to peak amplitude and frequency.
4) Vary the inductance in appropriate steps and record the frequency in each case.
5) Calculate the frequency theoretically and record it in the table. Compare the theoretical and practical values.

Observations:-

DC conditions:-

V_{BE} = ……. V_{CE} = ……

I_B = …… I_C = ……..

Sl. No.	Inductance (μH)	Frequency (Practically) (KHz)	Frequency $f_o = \frac{1}{2\pi} \times \sqrt{\frac{1}{L}(\frac{1}{C_1} + \frac{1}{C_2})}$

Result:-

Colpitts oscillator circuit is designed for the given specifications and its operation is studied.

EXPERIMENT NO: 9

HARTLEY OSCILLATOR

Aim:

To design and study the operation of Hartley Oscillator using BJT and determine the frequency of oscillation.

Components:

Name	Quantity
Transistor BC547	1
Resistor 74KΩ, 15 KΩ, 4.7KΩ, 1KΩ,	1,1,1,1
Capacitor 4.7μF, 100 PF	2, 1
Inductor 70 μH	2

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1

Digital Ammeter, Voltmeter	[0-200μA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BC 547:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:-

An oscillator is an electronic circuit that provides an AC output without using any AC input. All Sinusoidal oscillator circuits use the concept of positive feedback to produce oscillations. An oscillator circuit must satisfy the Barkhausen's criterion of unity loop gain to produce oscillations.

Hartley's oscillator is a popular LC Oscillator circuit used at Radio Frequencies.

Design:

Q: Design Hartley's oscillator circuit to provide oscillations at a frequency of 850 KHz. Use BJT BC547 for which β = 200, h_{fe} = 50, h_{ie} = 1.5 KΩ and $V_{BE(active)}$ = 0.65V. The biasing conditions are as follows.V_{CC} = 12V, I_C = 1mA, V_{CE} = 6V and Stability factor is S = 10. Use R_C = 4.7KΩ.

Solution:

Use, $I_C = \beta \times I_B$

$$\Rightarrow I_B = 5\mu A$$

Apply KVL to the output loop:

$$-V_{CC} + I_C \times R_C + V_{CE} + I_C \times R_E = 0$$

$$\Rightarrow R_E = 1.3K\Omega$$

Apply Thevenin's theorem to the base circuit, then

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \text{ And } R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1+\beta}{1+\frac{\beta \times R_E}{R_B + R_E}}$$

$$\Rightarrow R_B = 12.31K\Omega$$

Apply KVL to the input loop, then

$$-V_B + I_B \times R_B + V_{BE} - I_E \times R_E = 0$$

$$\Rightarrow V_B = 2.01\text{V}$$

Divide R_B with V_B:

$$\Rightarrow R_1 = \frac{V_{CC} \times R_B}{V_B} = 73.5K\Omega$$

Also, $R_B = \dfrac{R_1 \times R_2}{R_1 + R_2} \quad \Rightarrow R_2 = 14.8K\Omega$

Assume that $L_1 = L_2 = 70\mu H$ and $M = 45\mu H$. Then $C = 100$ PF.

We know that $f_o = \dfrac{1}{2\pi\sqrt{(L_1 + L_2 + 2M)C}}$

Circuit diagram:-

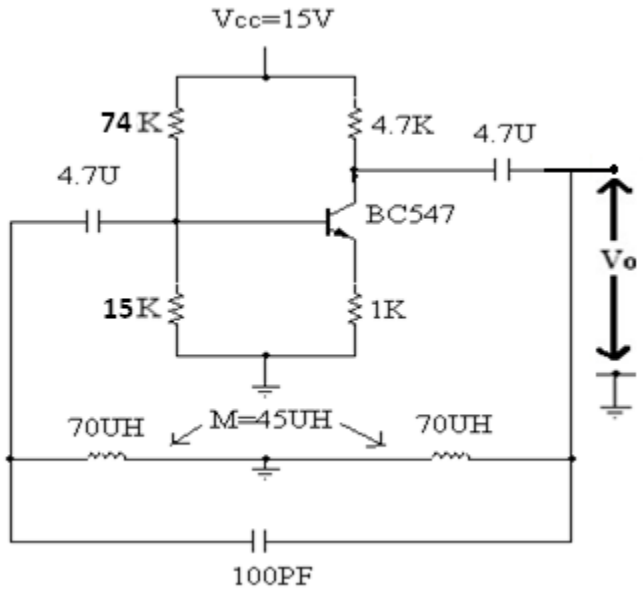


Fig (1): Hartley's Oscillator

Procedure:-

1) Connect the self bias circuit and check the DC conditions.
2) Connect other components of the oscillator circuit as shown in figure. Adjust the capacitance to 800 PF.
3) Observe the output voltage waveform on CRO screen. Note down its peak to peak amplitude and frequency.
4) Vary the capacitance in appropriate steps and record the frequency in each case.
5) Calculate the frequency theoretically also and record it in the table. Compare the theoretical and practical values.

Observations:-

DC conditions:-

V_{BE} = ……. V_{CE} = …….

I_B = …… I_C = ……..

Sl. No.	Capacitance (PF)	Frequency (Practically) (MHz)	Frequency $f_o = \frac{1}{2\pi\sqrt{(L_1 + L_2 + 2M)C}}$

Result:-

Hartley oscillator circuit is designed for the given specifications and its operation is studied.

EXPERIMENT NO: 10

SINGLE TUNED AMPLIFIER

Aim:-

To design and plot the frequency response of a single tuned amplifier.

Components:

Name	Quantity
Transistor BF194	1
Resistor 94KΩ, 68KΩ, 3.9KΩ, 2.2KΩ	1,1,1,1
Capacitor 10µF,100µF, 3.18 ηF	2, 1,1
Inductor 39 µH	1

Equipment:

Name	Range	Quantity

Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200μA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BF 194:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:-

Tuned amplifier circuit uses parallel LC resonant circuit as the load impedance, They have a very narrow bandwidth, hence they select a particular frequency and rejects other, they are used in radio receivers.

A single tuned amplifier consists of only one LC section as a load.

Design: -

Design a single tuned amplifier to provide a gain of 100 at a frequency of 455 KHZ and provide a bandwidth of 20 KHZ. Use transistor BF194 for which β = 90, g_m = 40mS. The biasing conditions are as follows. V_{CC} = 12V, V_{CE} = 8V, IC = 1mA and S = 10.

Sol:

Use, $I_C = \beta \times I_B$, $\Rightarrow I_B = 11.11\mu A$

Apply KVL to the output loop:

$$-V_{CC} + V_{CE} + I_C \times R_E = 0$$

$$\Rightarrow R_E = 4K\Omega \cong 3.9K\Omega$$

Apply Thevenin's theorem to the base circuit, then

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \quad \text{And} \quad R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1+\beta}{1+\frac{\beta \times R_E}{R_B + R_E}}$$

$$\Rightarrow R_B = 39.43K\Omega$$

Apply KVL to the input loop, then

$$-V_B + I_B \times R_B + V_{BE} - I_E \times R_E = 0$$

$$\Rightarrow V_B = 5V$$

Divide R_B with V_B:

$$\Rightarrow R_1 = \frac{V_{CC} \times R_B}{V_B} = 94.63K\Omega$$

Also, $R_B = \frac{R_1 \times R_2}{R_1 \div R_2} \qquad \Rightarrow R_2 = 68K\Omega$

Circuit diagram:-

Design of tuned circuit:-

Effective quality factor is given by

$$Q_e = \frac{f_o}{BW} = 22.75$$

We know that the gain of a single tuned amplifier at resonant frequency is given by,

$$|A_{res}| = g_m \varpi_o L Q_e$$

$$\Rightarrow L = 38.44\mu H$$

Also the resonant frequency of the single tuned amplifier is given by,

$$\varpi_o = \frac{1}{\sqrt{LC}}$$

$$\Rightarrow C = \frac{1}{\varpi_o^2 \times L} = 3.183nF$$

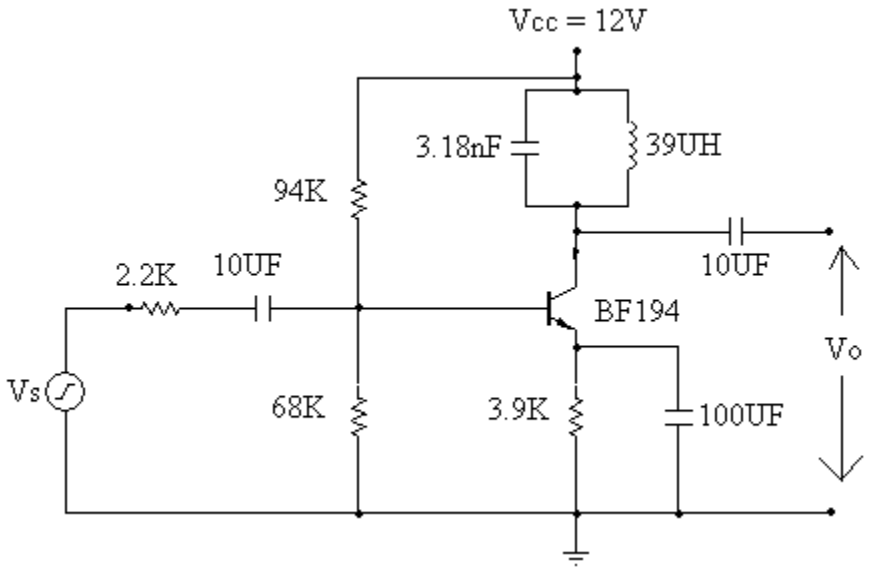


Fig (1): Single tuned amplifier

Procedure:-

1) Connect the self bias circuit and check the DC conditions.
2) Connect the other components and set the generator frequency at 455KHZ. Adjust the peak to peak amplitude of the input voltage to 30mV. Observe the output voltage waveform on the CRO screen and note the peak to peak value of the output voltage. Calculate the gain.
3) Vary the frequency from 400 to 600KHZ in appropriate steps.
4) Calculate the gain for each frequency.
5) Plot a graph between gain and frequency. Calculate bandwidth from the graph.

Observations:-

DC conditions:-

V_{BE} = ……. V_{CE} = ……

I_B = …… I_C = ……..

Frequency Response:-

Sl. No.	Frequency	V_i (mV)	V_o (V)	Gain = $\frac{Vo}{Vi}$

Expected Graph:-

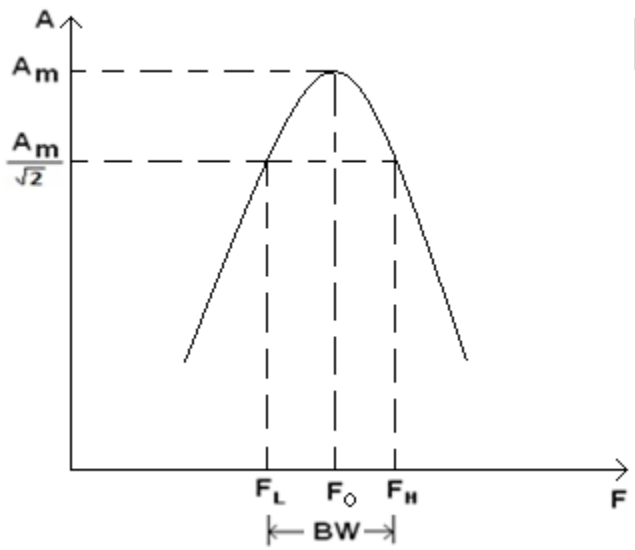


Fig (2): Frequency response of single tuned amplifier

Result:-

Resonant frequency = ----------

Gain at resonance = ----------

Bandwidth = ----------

EXPERIMENT NO: 11

DOUBLE TUNED AMPLIFIER

Aim:-

To design and plot the frequency response of a double tuned amplifier.

Components:

Name	Quantity
Transistor BF194	1
Resistor 94KΩ, 68KΩ, 3.9KΩ, 2.2KΩ	1,1,1,1
Capacitor 10µF,100µF, Capacitance box	2, 1,1
Inductance box	1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual DC power supply	0-30V	1
Function Generator	(0-1)MHz	1
Digital Ammeter, Voltmeter	[0-200µA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Specifications:

For Transistor BF 194:

- Max Collector Current= 0.1A
- V_{ceo} max= 50V
- V_{EB0} = 6V
- V_{CB0} = 50V
- Collector power dissipation = 500mW
- Temperature Range = -65 to +150 ^{0}C
- h_{fe} = 110 - 220

Theory:-

Tuned amplifier circuit uses parallel LC resonant circuit as the load impedance, They have a very narrow bandwidth, hence they select a particular frequency and rejects other, they are used in radio receivers.

A double tuned amplifier consists of two LC sections as a load.

Design:-

Design a double tuned amplifier to provide maximum gain at a frequency of 350KHz. Use transistor BF194 for which $\beta = 90$, $g_m = 40mS$.

The biasing conditions are as follows. $V_{CC} = 12V$, $V_{CE} = 8V$, IC = 1mA and S = 10.

Sol:-

Use, $I_C = \beta \times I_B$, $\Rightarrow I_B = 11.11\mu A$

Apply KVL to the output loop:

$$-V_{CC} + V_{CE} + I_C \times R_E = 0$$

$$\Rightarrow R_E = 4K\Omega \cong 3.9K\Omega$$

Apply Thevenin's theorem to the base circuit, then

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} \quad \text{And} \quad R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1+\beta}{1+\frac{\beta \times R_E}{R_B + R_E}}$$

$$\Rightarrow R_B = 39.43K\Omega$$

Apply KVL to the input loop, then

$$-V_B + I_B \times R_B + V_{BE} - I_E \times R_E = 0$$

$$\Rightarrow V_B = 5V$$

Divide R_B with V_B:

$$\Rightarrow R_1 = \frac{V_{CC} \times R_B}{V_B} = 94.63K\Omega$$

Also, $R_B = \frac{R_1 \times R_2}{R_1 \div R_2}$ $\Rightarrow R_2 = 68K\Omega$

Design of tuned circuit:-

An Intermediate Frequency Transformer with a centre frequency of 350 KHz is used.

Circuit diagram:-

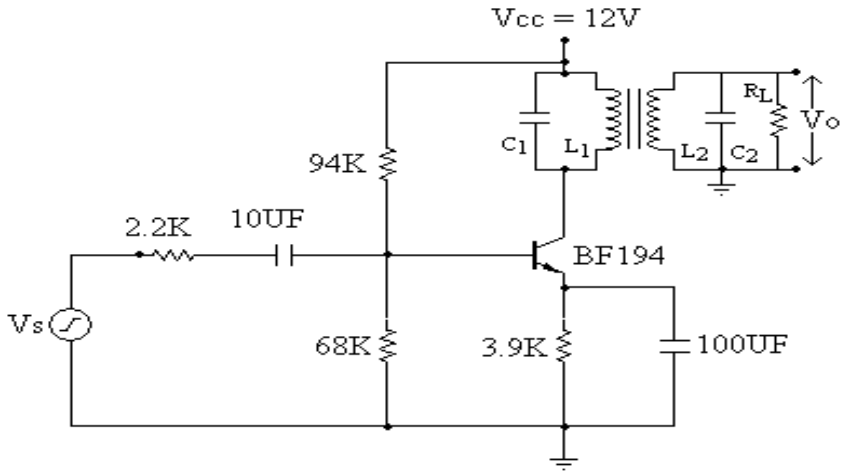


Fig (1): Double tuned amplifier

Procedure:-

1) Connect the self bias circuit and check the DC conditions.
2) Connect the other components and set the generator frequency at 350KHZ. Adjust the peak to peak amplitude of the input voltage to 30mV. Observe the output voltage waveform on the CRO screen and note the peak to peak value of the output voltage. Calculate the gain.
3) Vary the frequency from 250 to 500KHZ in steps of 10KHz and record V_i, V_o in every step.
4) Calculate the gain for each frequency.
5) Plot a graph between gain and frequency. Calculate bandwidth from the graph.

Observations:-

DC conditions:-

V_{BE} = ……. V_{CE} = ……

I_B = …… I_C = ……..

Frequency Response:-

Sl. No.	Frequency	V_i (mV)	V_o (V)	Gain = $\frac{Vo}{Vi}$

Expected Graph:-

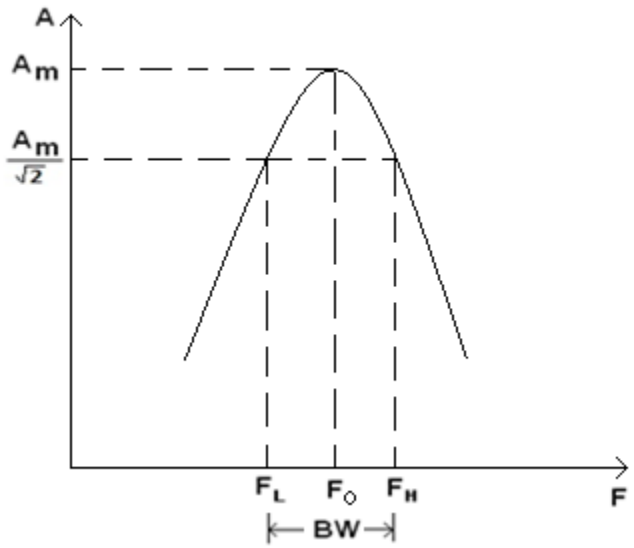


Fig (2): Frequency response of double tuned amplifier

Result:-

Resonant frequency = ----------

Gain at resonance = ----------

Bandwidth = ----------

Experiment no: 12

Constant K Low Pass Filter.

Aim:-

1) To design a T-section constant K Low Pass Filter with a cut-off frequency of 2 KHz and a characteristic load impedance of 600Ω.

2) To obtain the output characteristics of the above filter.

Components:

Name	Quantity
Resistor 600Ω	1
Capacitance box	1
Inductance box	2

Equipment:

Name	Range	Quantity
Bread Board		1
Function Generator	(0-2)MHz	1
Digital Ammeter, Voltmeter	[0-200μA/200mA], [0-20V]	1
CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Theory:-

Low pass filter is a circuit which passes low frequency signals and attenuates high frequency signals,

The frequency at which the gain is 70% of the maximum value is called as cut off frequency.

Design:-

We know that the cut off frequency is given by,

$$f_C = \frac{1}{\pi\sqrt{LC}}$$

and the characteristic load impedance is, $R_K = \sqrt{\frac{L}{C}}$

then the design equations for L and C will be

$$L = \frac{R_K}{\pi f_C} = \frac{600}{\pi \times 2000} = 48mH$$

$$C = \frac{1}{\pi R_K f_C} = \frac{1}{\pi \times 600 \times 2000} = 0.26\mu F$$

Circuit Diagram:-

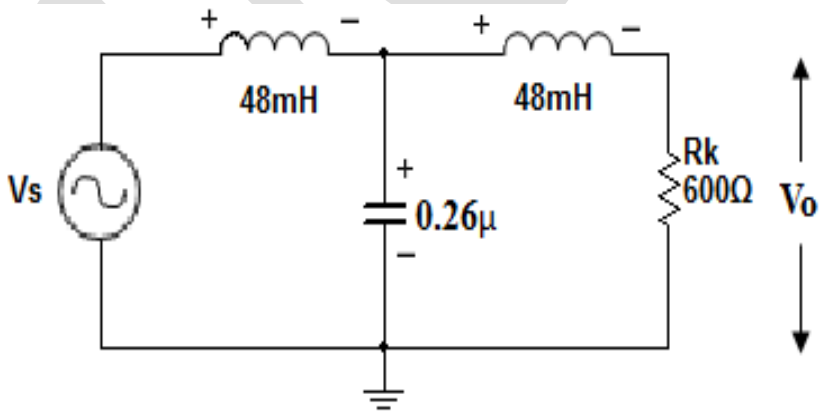


Fig (1): Low pass filter

Procedure:-

1) Connect the components as shown in the circuit diagram.
2) Adjust V_i = 4V (peak-to-peak) and keep it constant throughout the experiment.

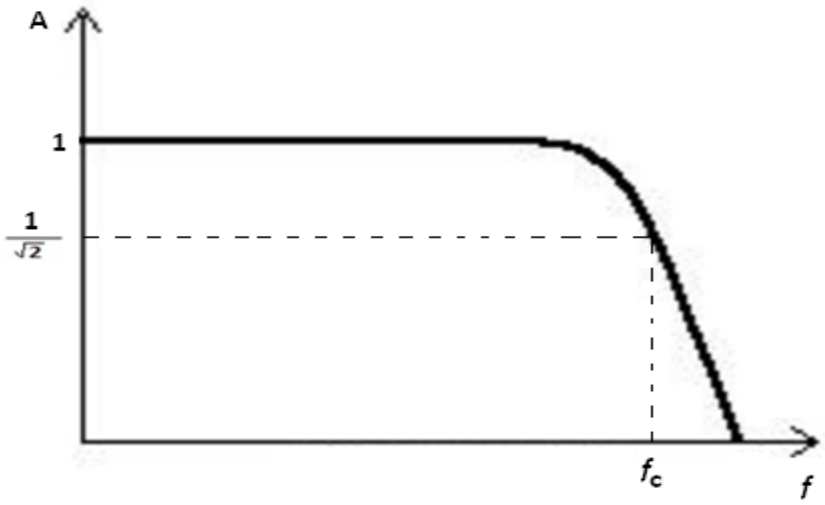
3) Vary the input frequency from 100 Hz to 20 Khz in steps of 200 Hz and note down the peak-to-peak voltage across R_L i.e., V_O.

Note: Take more readings between 1.8KHz and 2.2KHz.

4) Plot the variation of Gain Versus frequency

5) From the graph find out f_C.

Expected Graphs:-



Fig(2): Frequency response of low pass filter

Observations:-

Sl. No.	**Frequency (Hz)**	**V_i (Volt)**	**V_O (Volt)**	**A = $\frac{V_O}{V_i}$**	$\alpha = \ln\left(\frac{V_i}{V_O}\right)$

Results:-

From the attenuation characteristics curve,

$f_C = ...Hz$

Experiment no: 13

m-Derived High Pass Filter

Aim:-

1) To design an m-derived high pass T-section filter with a cut-off frequency of 1.2 KHz, characteristic load impedance of 600 Ω and $f_\infty = 1.1KHz$

2) To obtain output characteristics of the above filter.

Components:

Name	Quantity
Resistor 600Ω	1
Capacitance box	3
Inductance box	1

Equipment:

Name	Range	Quantity
Bread Board		1
Function Generator	(0-2)MHz	1
Digital Ammeter, Voltmeter	[0-200μA/200mA], [0-20V]	1

CRO	(0-20)MHz	1
CRO probes, Connecting Wires		

Theory:-

High pass filter is a circuit which passes high frequency signals and attenuates low frequency signals,

The frequency at which the gain is 70% of the maximum value is called as cut off frequency.

m-derived filters have a very sharp cut off frequency

Design:-

a) Design of prototype High Pass T-section

$$L = \frac{R_O}{4\pi f_C} = \frac{600}{4\pi \times 1200} = 39.78mH$$

$$C = \frac{1}{4\pi R_O f_C} = \frac{1}{4\pi \times 600 \times 1200} = 0.11\mu F$$

Value of m for m-derived section to give infinite attenuation at 1100 Hz is given by,

$$m = \sqrt{1-\left(\frac{f_\infty}{f_C}\right)^2} = \sqrt{1-\left(\frac{1100}{1200}\right)^2} = 0.4$$

b) for the m-derived T-section

Each series arm $= \frac{2C}{m} = \frac{0.22}{0.4} = 0.55\mu F$

Shunt arm $= \frac{L}{m} = \frac{39.78}{0.4} = 99.45mH$

And, $\frac{4mC}{1-m^2} = \frac{4 \times 0.4 \times 0.11}{1-(0.4)^2} = 0.21\mu F$

Circuit Diagram:-

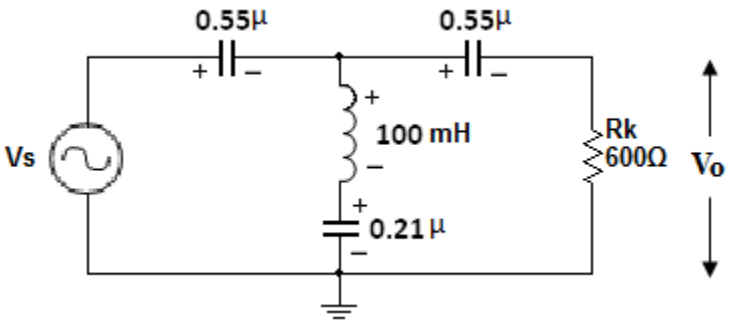


Fig (1): High pass filter

Procedure:-

1) Connect the components as shown in the circuit diagram.
2) Adjust V_i = 4V (peak-to-peak) and keep it constant throughout the experiment.
3) Vary the input frequency from 100 Hz to 20 Khz in steps of 200 Hz and note down the peak-to-peak voltage across R_L i.e., V_O.

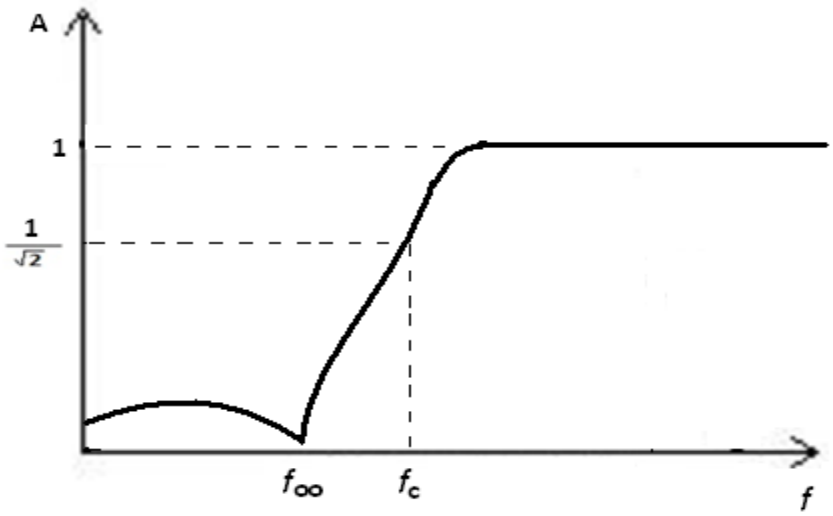
Note: Take more readings between 1.1KHz and 1.2KHz.

4) Plot the variation of Gain Versus frequency
5) From the graph find out f_C and f_∞.

Observations:-

Sl. No.	**Frequency (Hz)**	**V_i (Volt)**	**V_O (Volt)**	**A = $\frac{V_O}{V_i}$**	$\alpha = \ln\left(\frac{V_i}{V_O}\right)$

Expected Graphs:-



Fig(2): Frequency response of high pass filter

Results:-

From the attenuation characteristics curve,

$f_C = ...Hz$

$f_\infty = ...Hz$

APPENDIX

LABORATORY COURSE ASSESSMENT GUIDELINES

i. The number of experiments in each laboratory course shall be as per the curriculum in the scheme of instructions provided by OU. Mostly the number of experiments is 10 in each laboratory course under semester scheme and 18 under year wise scheme.

ii. The students will maintain a separate note book for observations in each laboratory course.

iii. In each session the students will conduct the allotted experiment and enter the data in the observation table.

iv. The students will then complete the calculations and obtain the results. The course coordinator will certify the result in the same session.

v. The students will submit the record in the next class. The evaluation will be continuous and not cycle-wise or at semester end.

vi. The internal marks of 25 are awarded in the following manner:
   a. Laboratory record - Maximum Marks 15
   b. Test and Viva Voce - Maximum Marks 10

vii. Laboratory Record: Each experimental record is evaluated for a score of 50. **The rubric parameters are as follows:**
   a. Write up format - Maximum Score 15
   b. Experimentation Observations & Calculations - Maximum Score 20
   c. Results and Graphs - Maximum Score 10
   d. Discussion of results - Maximum Score 5

While (a), (c) and (d) are assessed at the time of record submission, (b) is assessed during the session based on the observations and calculations. Hence if a student is absent for an experiment but completes it in another session and subsequently submits the record, it shall be evaluated for a score of 30 and not 50.

viii. The experiment evaluation rubric is therefore as follows:

Parameter	Max Score	Outstanding	Accomplished	Developing	Beginner	Points
Observations and Calculations	20					
Write up format	15					
Results and graphs	10					
Discussion of Results	5					

LABORATORY EXPERIMENT EVALUATION RUBRIC

CATEGORY	OUTSTANDING (Up to 100%)	ACCOMPLISHED (Up to 75%)	DEVELOPING (Up to 50%)	BEGINNER (Up to 25%)
Write up format	Aim, Apparatus, material requirement, theoretical basis, procedure of experiment, sketch of the experimental setup etc. is demarcated and presented in clearly labeled and neatly organized sections.	The write up follows the specified format but a couple of the specified parameters are missing.	The report follows the specified format but a few of the formats are missing and the experimental sketch is not included in the report	The write up does not follow the specified format and the presentation is shabby.
Observations and Calculations	The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures. One sample calculation is explained by substitution of values	The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures but sample calculation is not shown	The experimental observations and calculations are recorded neatly but correct units and significant figures are not used. Sample calculation is also not shown	The experimental observations and results are recorded carelessly. Correct units significant figures are not followed and sample calculations not shown
Results and Graphs	Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations are performed from the graphs. Equations are obtained by regression analysis or curve fitting if relevant	Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations from the graphs are incomplete and equations are not obtained by regression analysis or curve fitting	Results obtained are correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting	Results obtained are not correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting
Discussion of results	All relevant points of the result are discussed and justified in light of theoretical expectations. Reasons for divergent results are identified and corrective measures discussed.	Results are discussed but no theoretical reference is mentioned. Divergent results are identified but no satisfactory reasoning is given for the same.	Discussion of results is incomplete and divergent results are not identified.	Neither relevant points of the results are discussed nor divergent results identified

ix. The first page of the record will contain the following title sheet:

SAMPLE ASSESSMENT SHEET

NAME: **ROLL NO.**

Exp. No.	Date conducted	Date Submitted	Observations &Calculations (Max 20)	Write up (Max 15)	Results and Graphs (Max 10)	Discussion of Results (Max 5)	Total Score (Max 50)
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							

x. The 15 marks of laboratory record will be scaled down from the TOTAL of the assessment sheet.

xi. The test and viva voce will be scored for 10 marks as follows:

Internal Test	-	6 marks
Viva Voce / Quiz	-	4 marks

xii. Each laboratory course shall have 5 course outcomes.

The proposed course outcomes are as follows:

On successful completion of the course, the student will acquire the ability to:

1. Conduct experiments, take measurements and analyze the data through hands-on experience in order to demonstrate understanding of the theoretical concepts of _____, while working in small groups.

2. Demonstrate writing skills through clear laboratory reports.

3. Employ graphics packages for drawing of graphs and use computational software for statistical analysis of data.

4. Compare the experimental results with those introduced in lecture, draw relevant conclusions and substantiate them satisfactorily.

5. Transfer group experience to individual performance of experiments and demonstrate effective oral communication skills.

xiii. The Course coordinators would prepare the assessment matrix in accordance with the guidelines provided above for the five course outcomes. The scores to be entered against each of the course outcome would be the sum of the following as obtained from the assessment sheet in the record:

   a. Course Outcome 1: Sum of the scores under 'Observations and Calculations'.
   b. Course Outcome 2: Sum of the scores under 'Write up'.
   c. Course Outcome 3: Sum of the scores under 'Results and Graphs'.
   d. Course Outcome 4: Sum of the scores under 'Discussion of Results'.
   e. Course Outcome 5: Marks for 'Internal Test and Viva voce'.

xiv. Soft copy of the assessment matrix would be provided to the course coordinators.

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

Program Outcomes of B.E (ECE) Program:

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12: Life-long learning: Recognise the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs) of ECE Department, MJCET

PSO1: The ECE Graduates will acquire state of art analysis and design skills in the areas of digital and analog VLSI Design using modern CAD tools.

PSO2: The ECE Graduates will develop preliminary skills and capabilities necessary for embedded system design and demonstrate understanding of its societal impact.

PSO3: The ECE Graduates will obtain the knowledge of the working principles of modern communication systems and be able to develop simulation models of components of a communication system.

PSO4: The ECE Graduates will develop soft skills, aptitude and programming skills to be employable in IT sector.